

Fig. 1

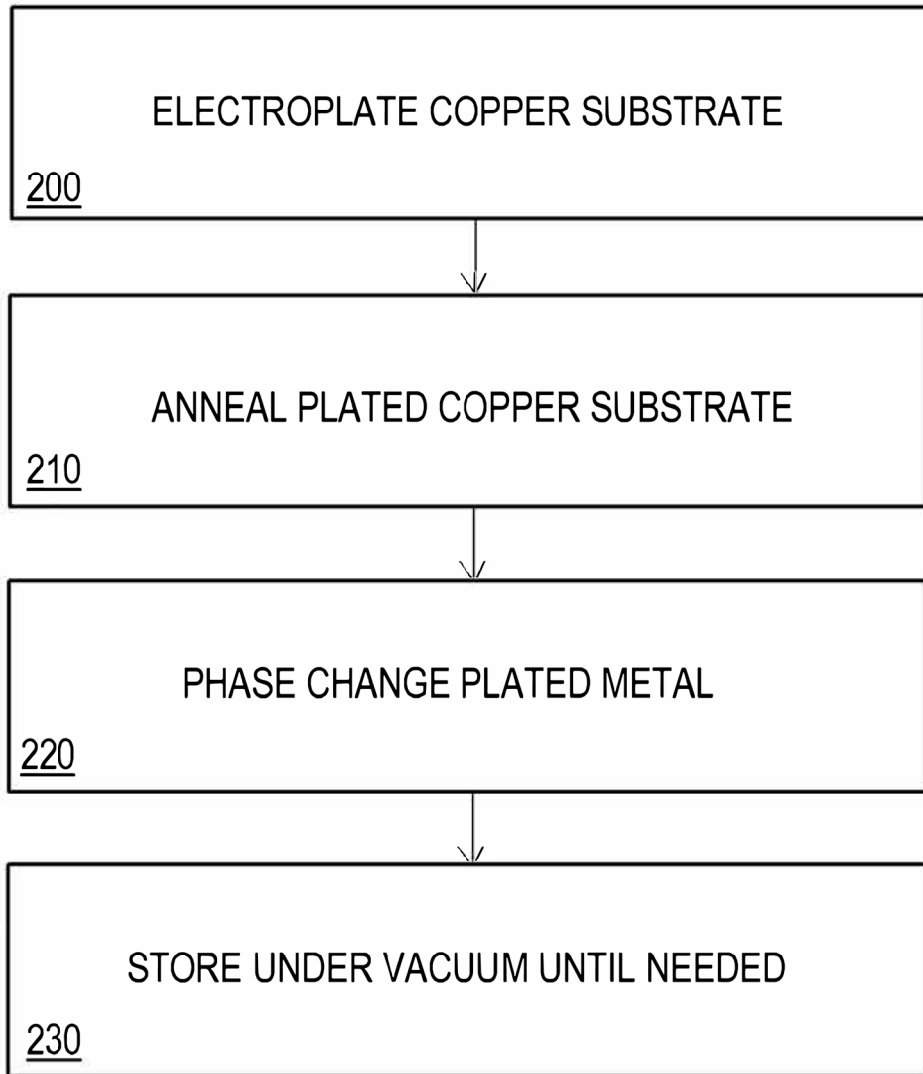


FIG. 2

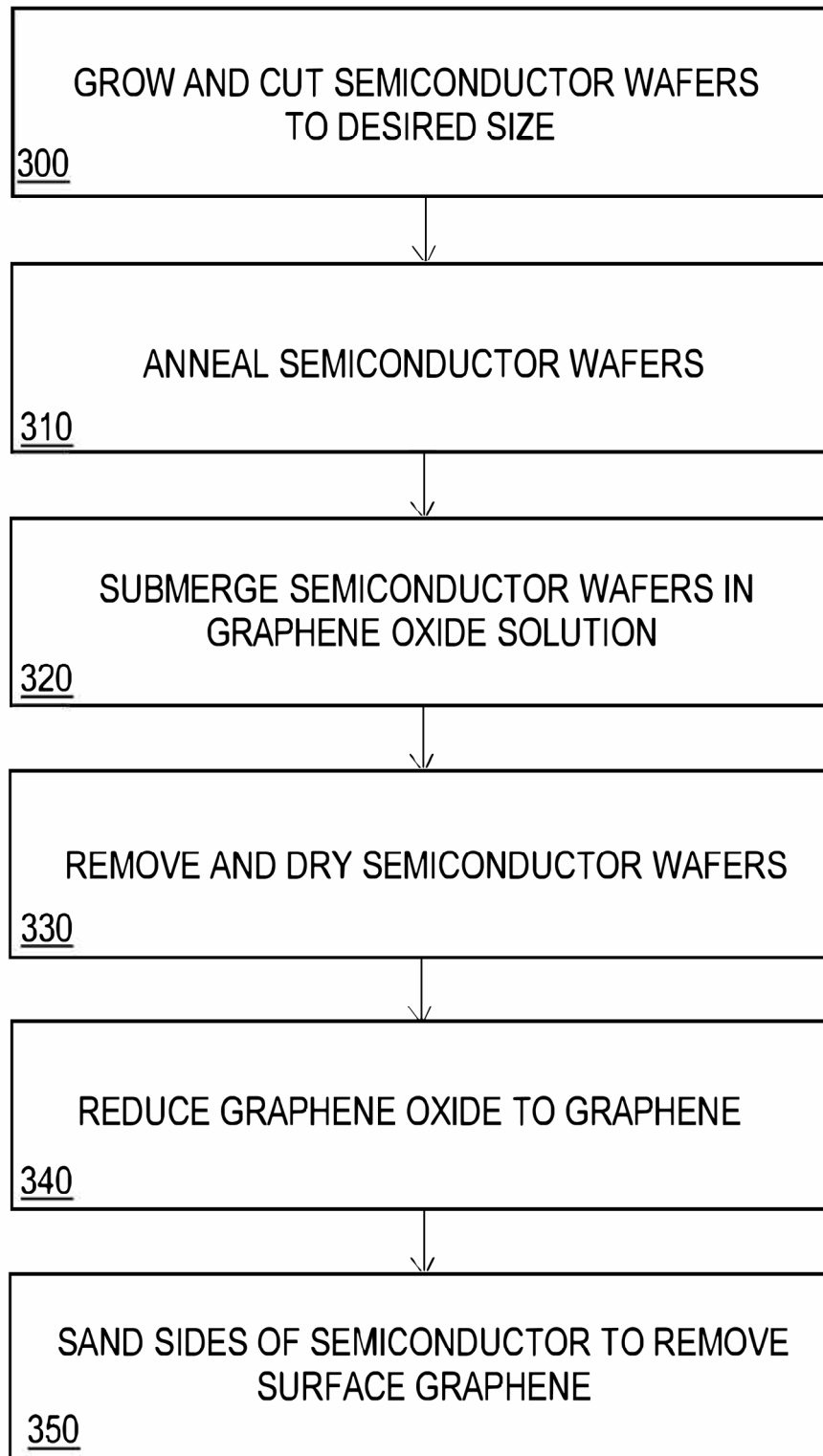


FIG. 3

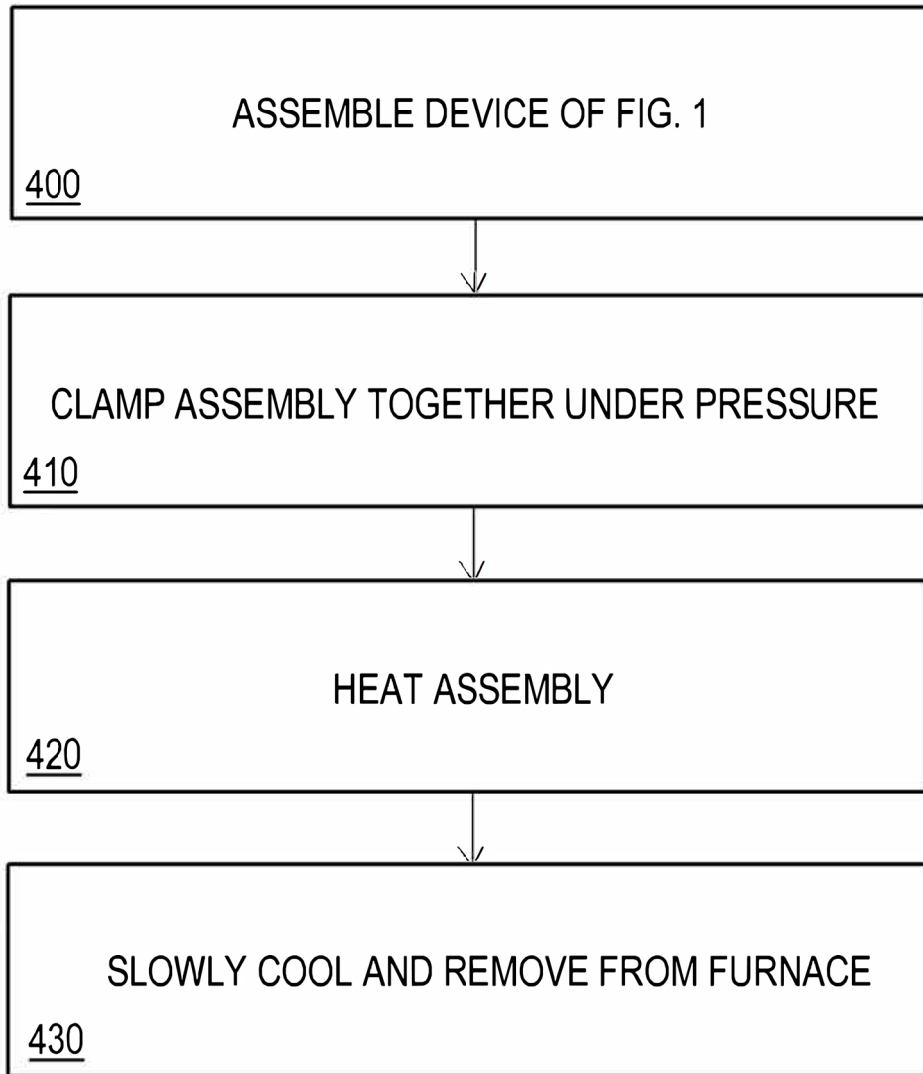


FIG. 4

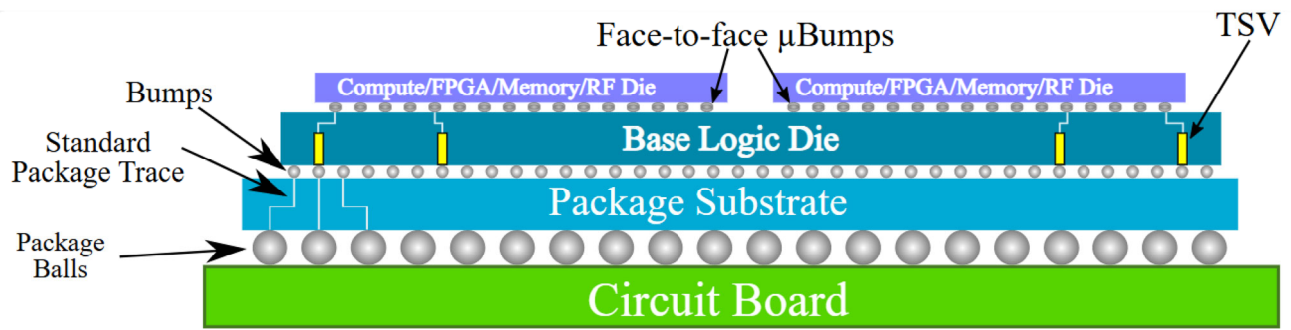


FIG. 5

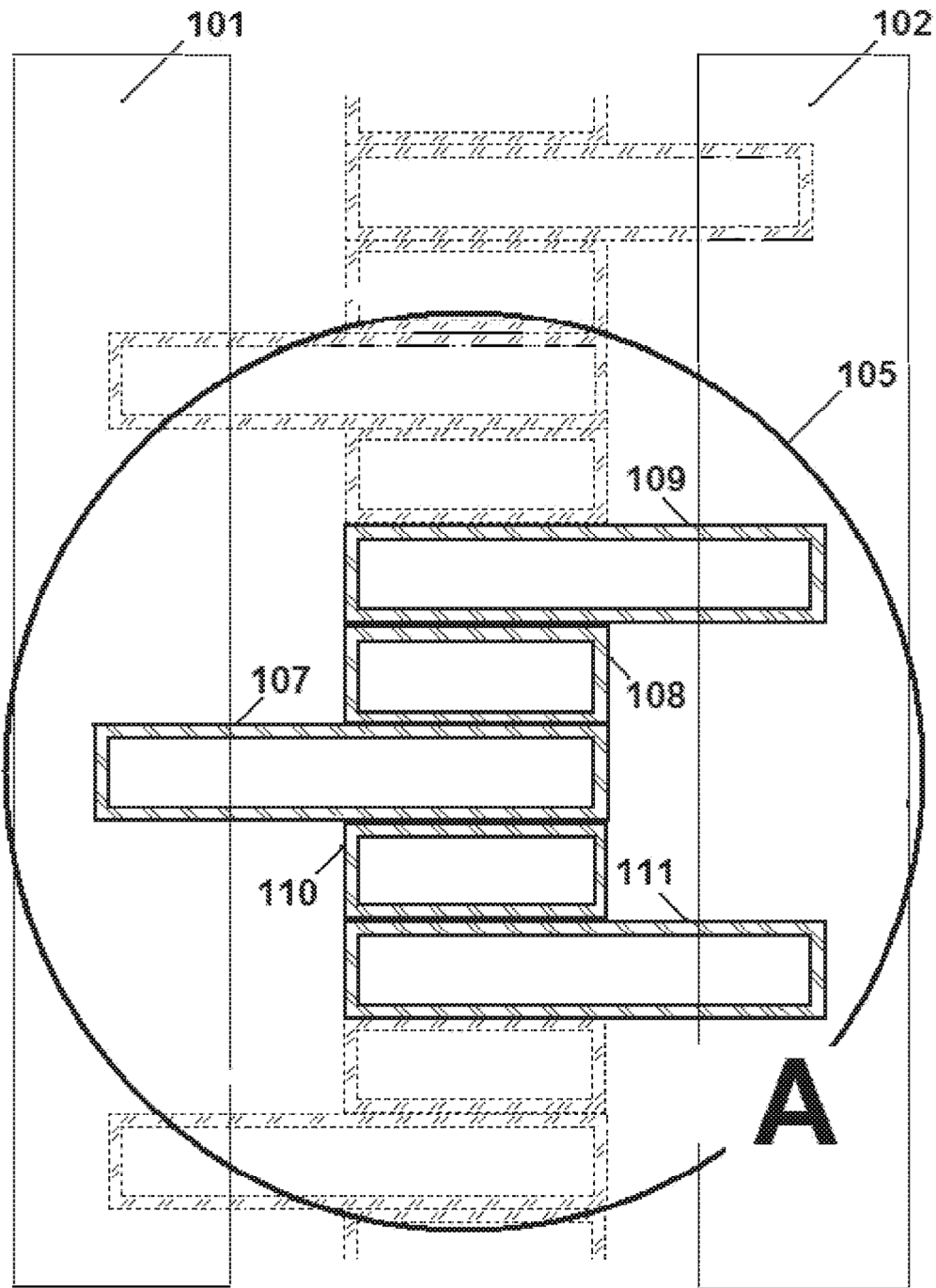


FIG. 6A

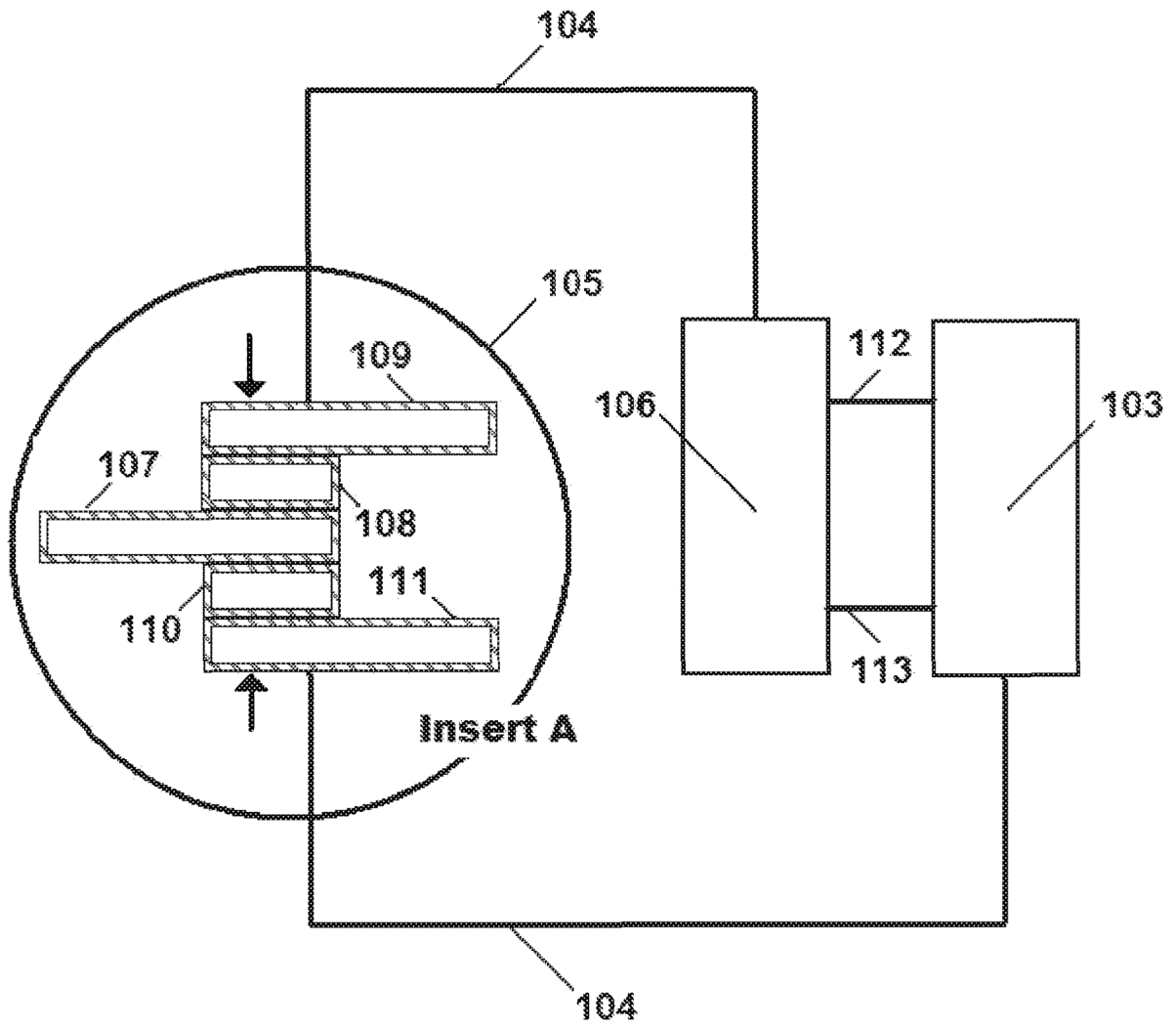


Fig. 6b

Fig. 7

**HOT AND COLD LAYERS
METAL BAR STOCK PROCESS**

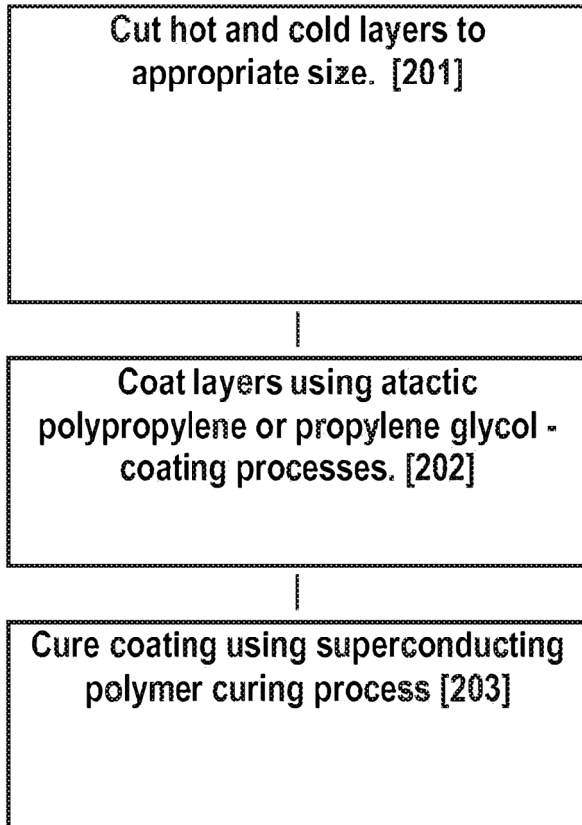


Fig. 8

**HOT AND COLD LAYERS
POWDER METAL PROCESS**

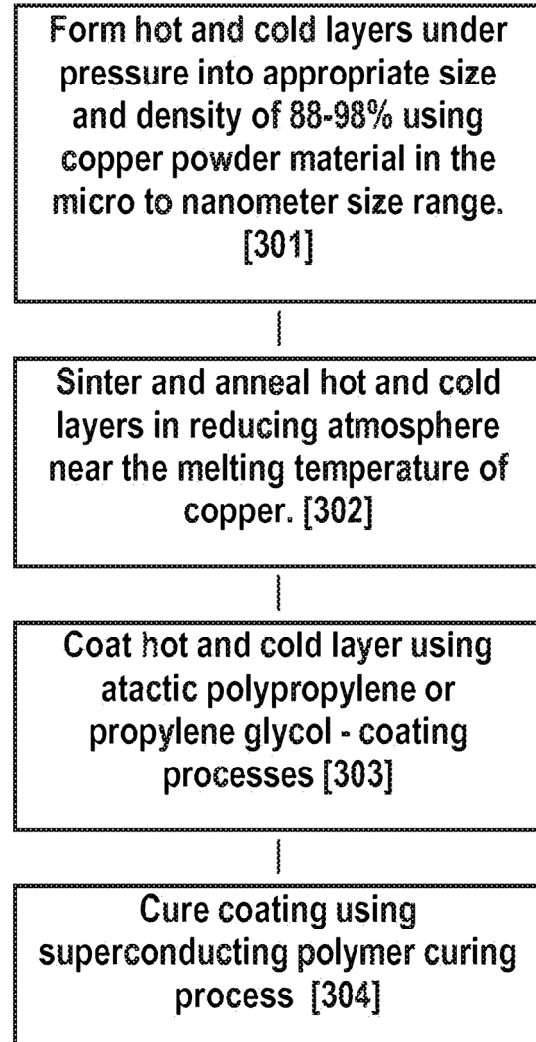


Fig. 9

HOT AND COLD LAYERS PROCESS WITH INTEGRAL SEMICONDUCTOR LAYER

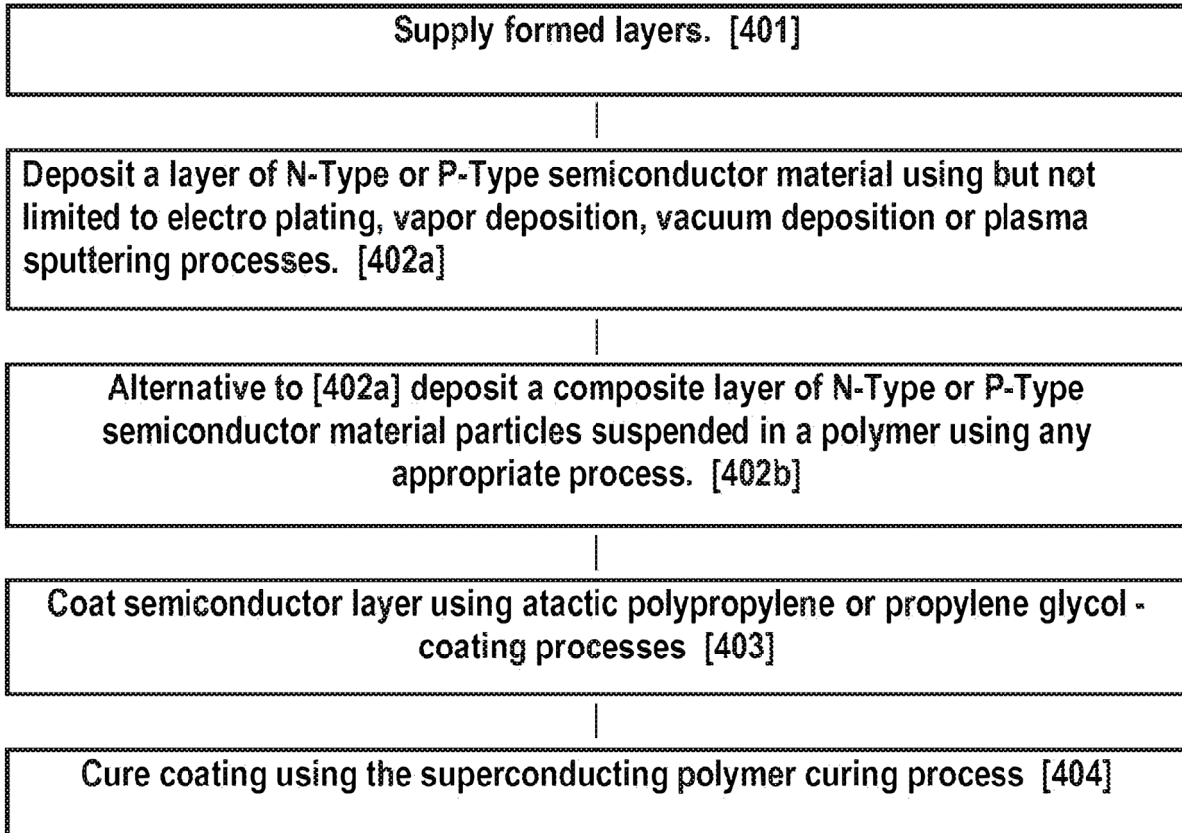


Fig. 10

SEMICONDUCTOR LAYER FORMATION - BRIDGEMAN MOLDING PROCESS

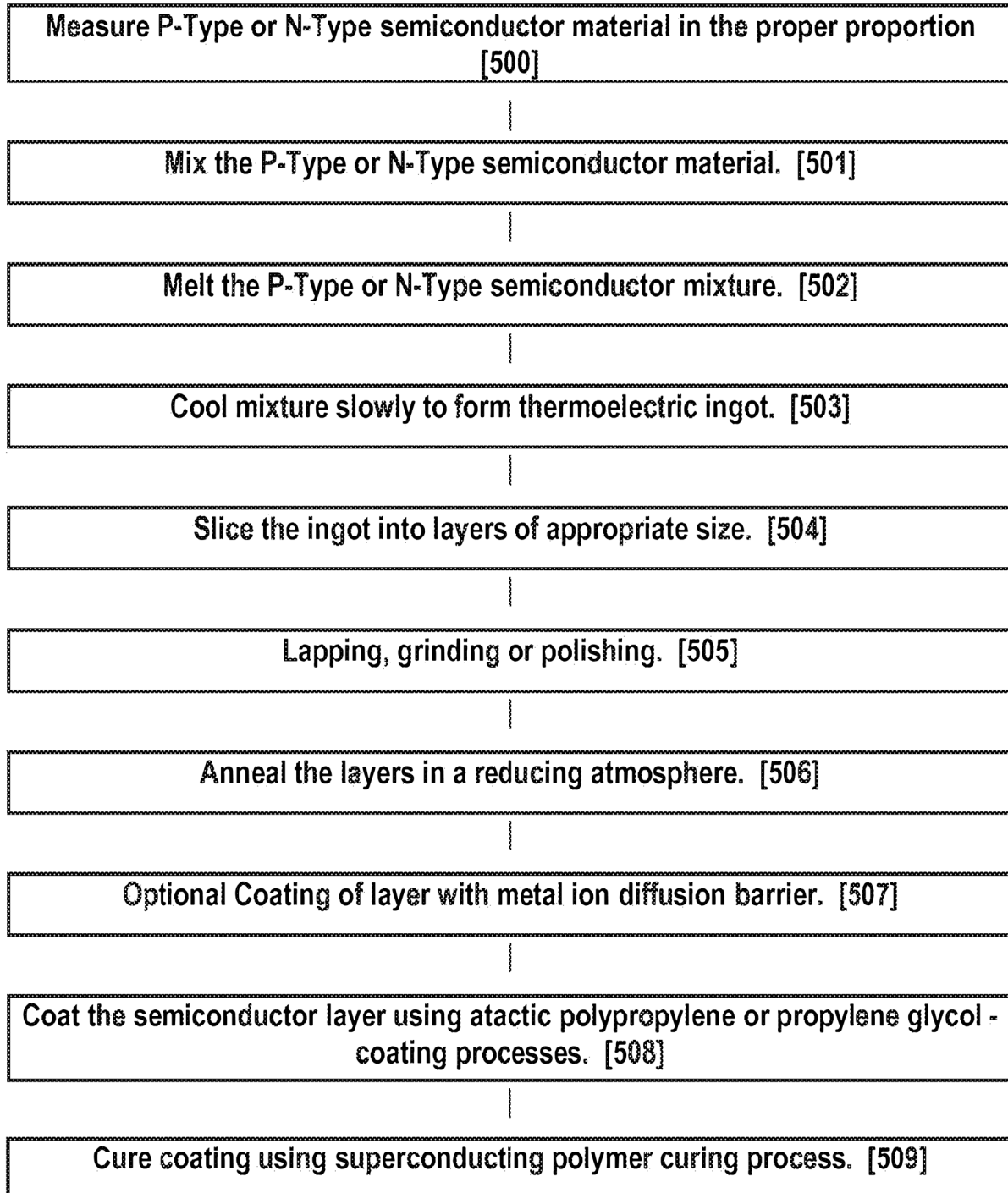


Fig. 11

**SEMICONDUCTOR LAYER FORMATION and CONCURRENT SUPERCONDUCTING
POLYMER COATING**

DIRECT MELTING PROCESS

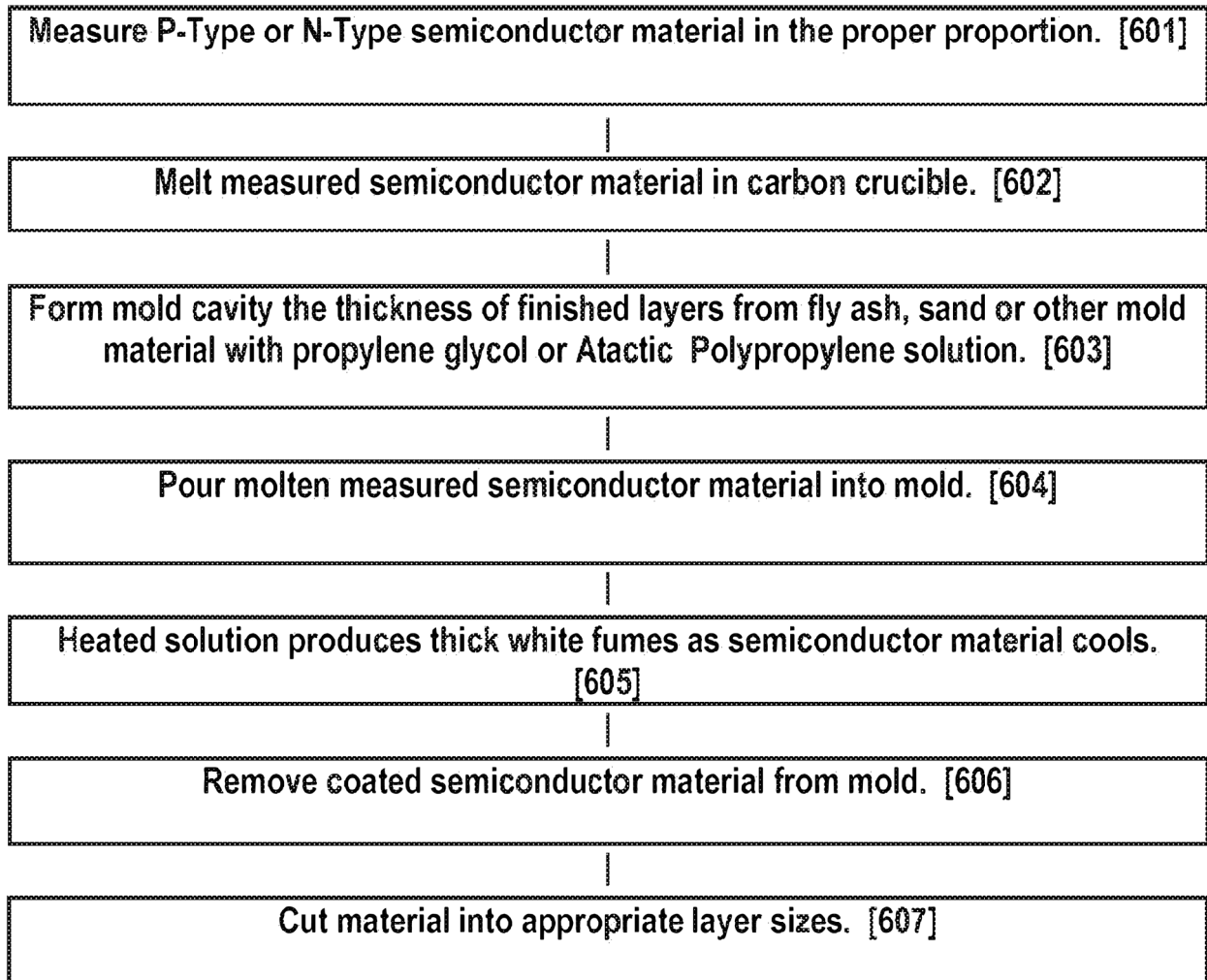


Fig. 12

SEMICONDUCTOR LAYER FORMATION

POWDERED METAL PROCESS

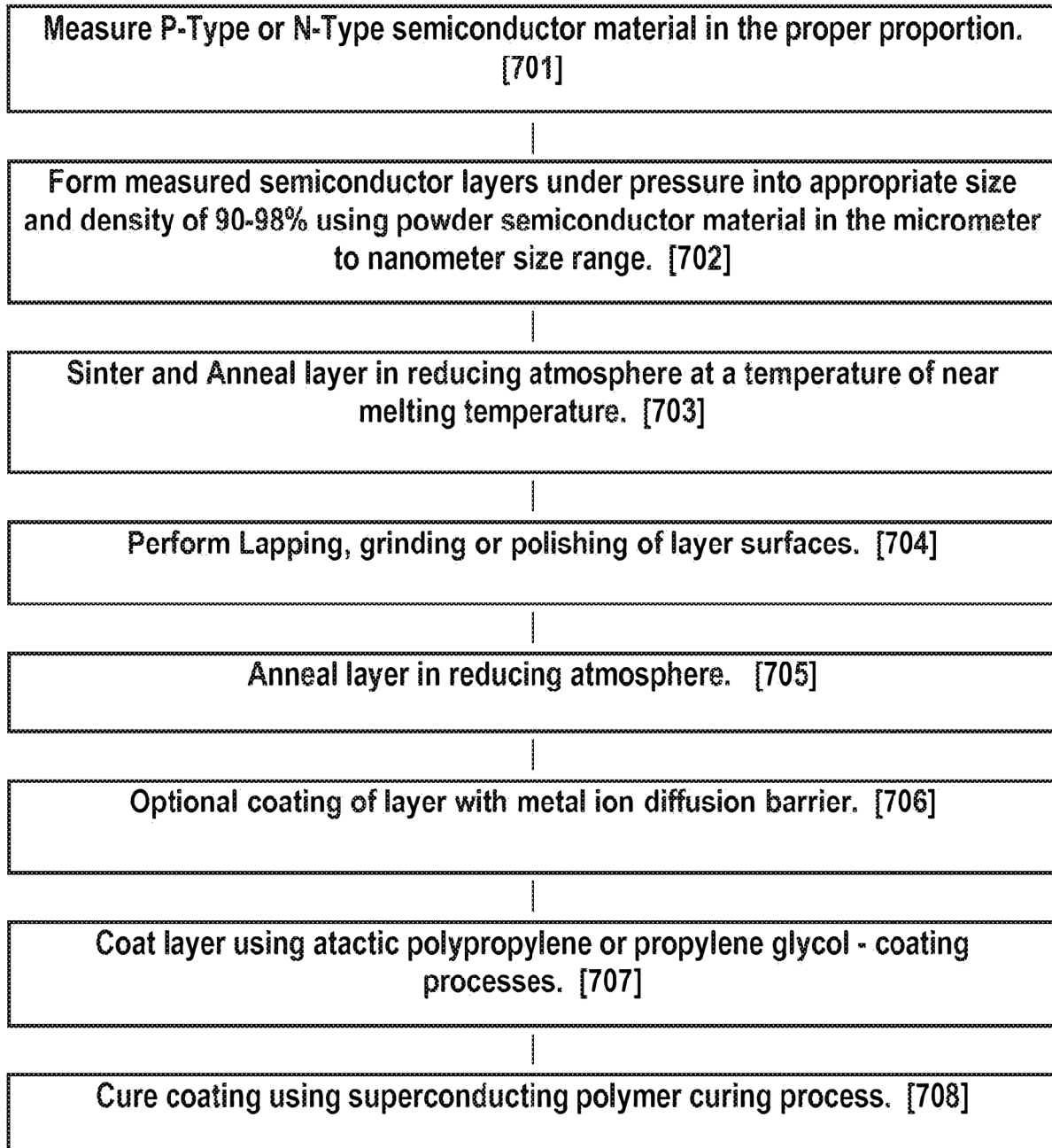


Fig. 13

**PROPYLENE GLYCOL
COATING PROCESS**

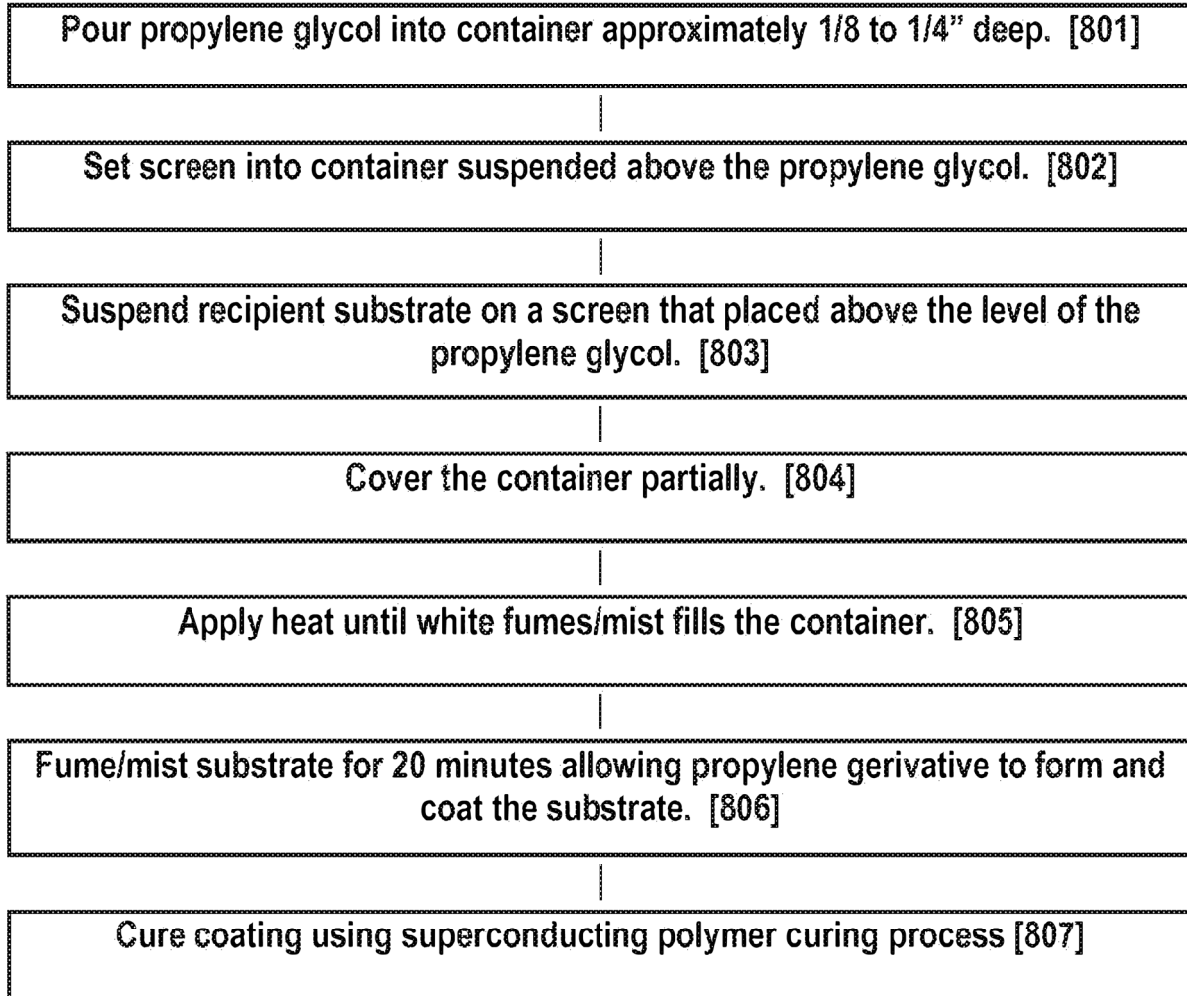


Fig. 14

**ATACTIC POLYPROPYLENE
COATING PROCESS**

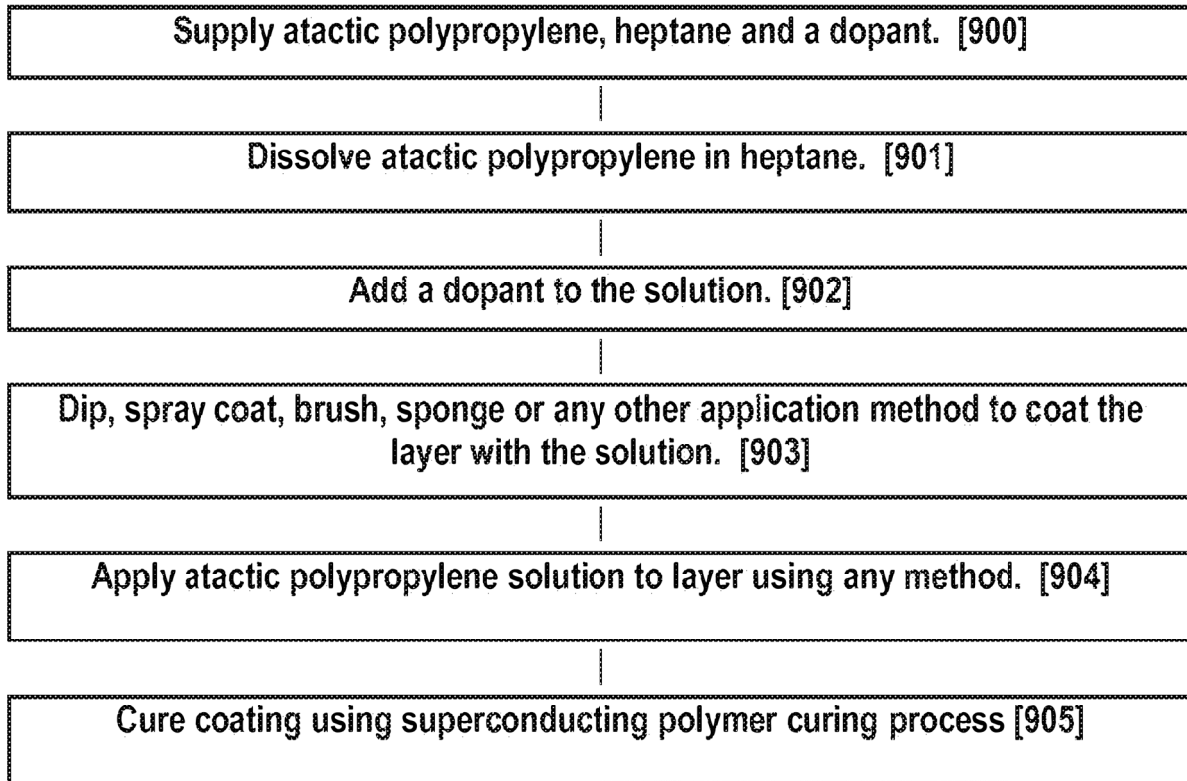


Fig. 15

**SUPERCONDUCTING POLYMER
CURING PROCESS**

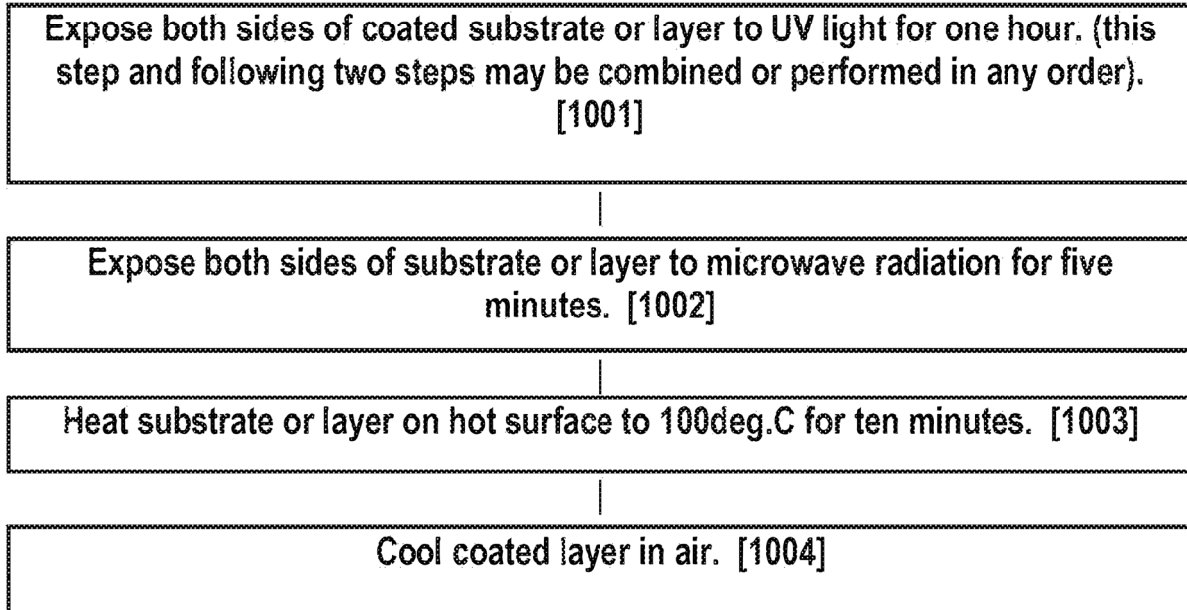


Fig. 16

**ELECTRIC FIELD CONDITIONING
ENERGY CONVERTER ASSEMBLLY**

(to insure superconductivity and electrical contact between layers and coatings)

Connect the negative terminal of a power source (DC power supply or pulse width modulator) to all of the hot layers and the positive terminal to all of the cold layers, placing the P-Type and N-Type semiconductors in a parallel electrical circuit. [1101]

Energize the power source for a time that is a function of the paramaters of the apparatus to condition the conductive paths. [1102]

Energize the power source with the terminals reversed for a time that is a function of the paramaters of the apparatus to condition the semiconductor paths. [1103]

Confirm conditioning of entire apparatus by measuring its conductivity with the parallel circuit removed. [1104]

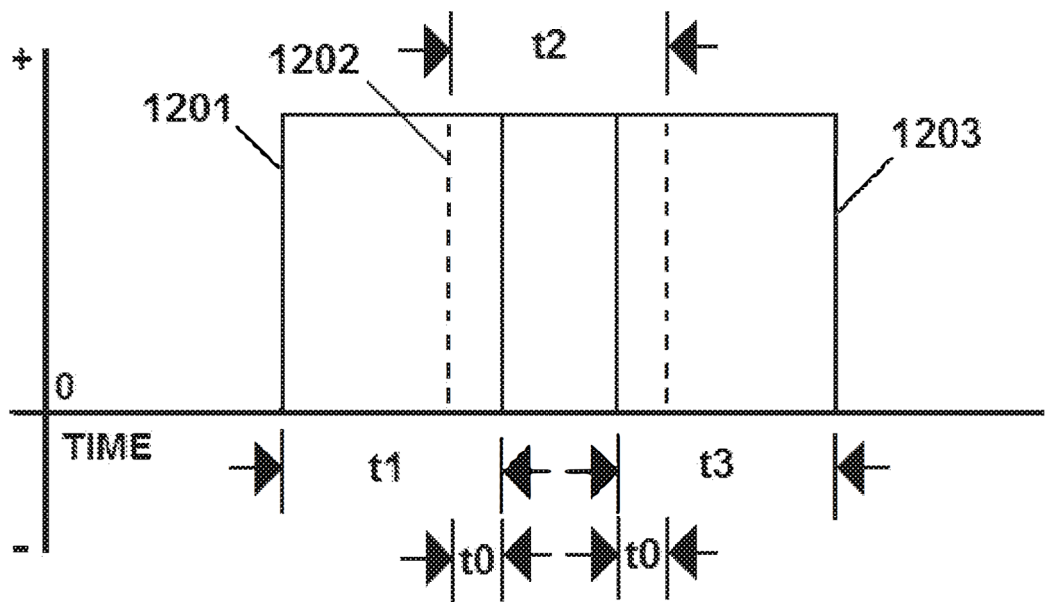


Fig. 17a

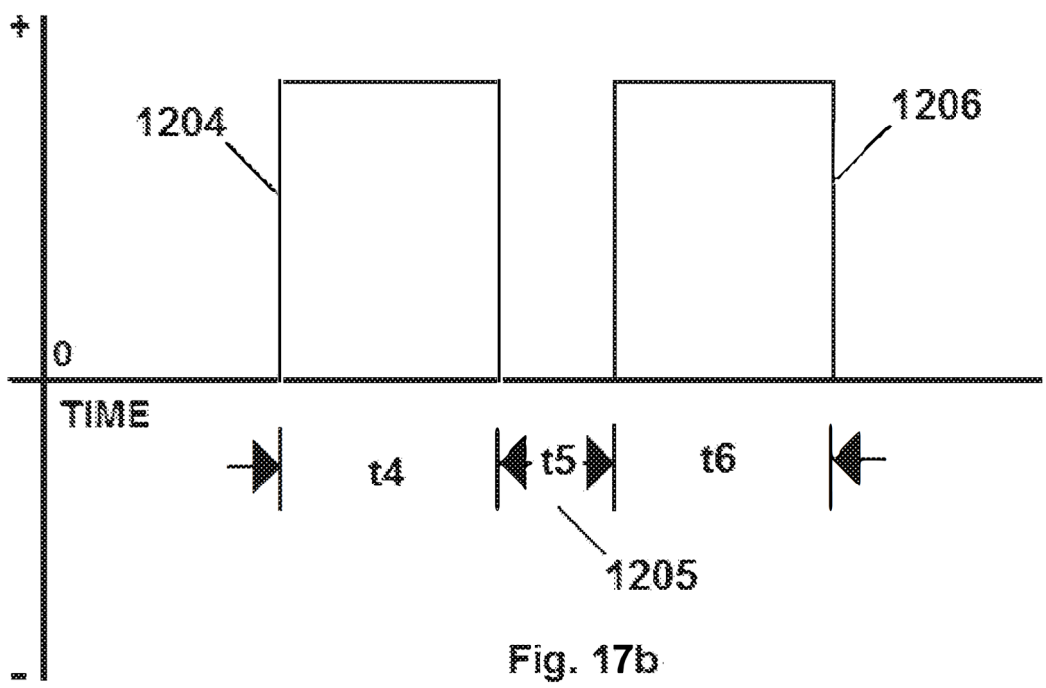


Fig. 17b

Fig. 18
PROCESS FOR COATING LAYERS
WITH SUPERCONDUCTING PASTE

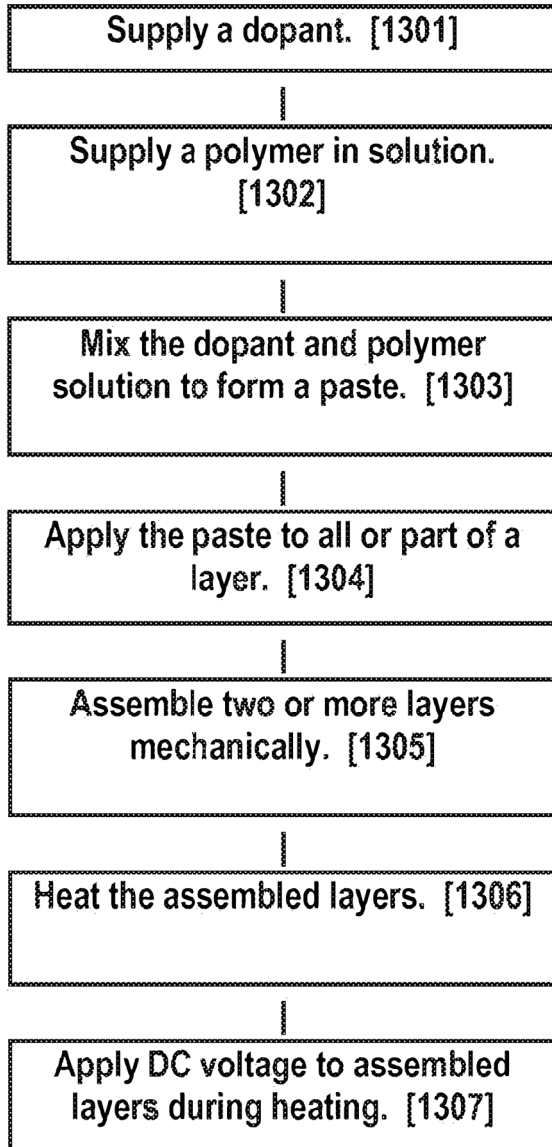


Fig. 19
ELECTRO-DEPOSITION
PROCESS FOR COATINGS OF
SUPERCONDUCTING POLYMERS

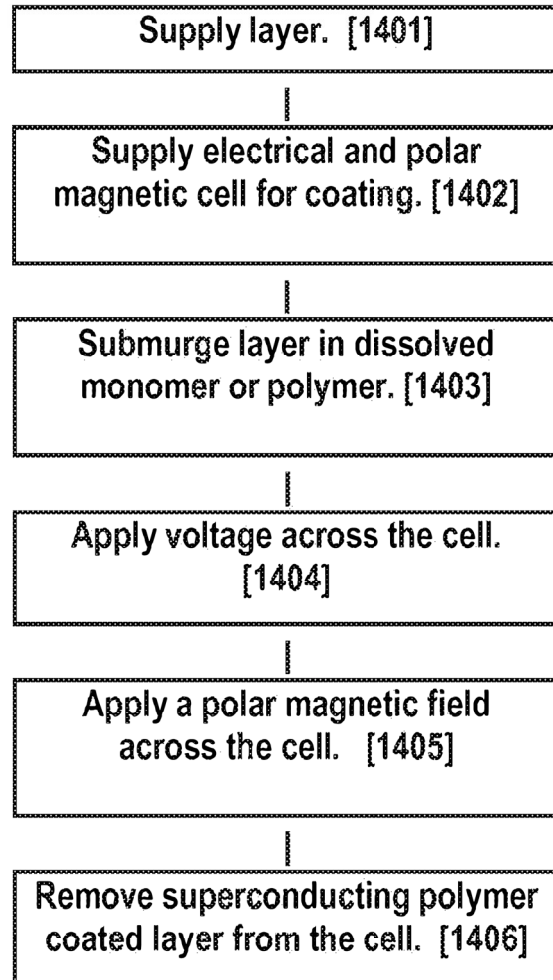


Fig. 20

**SUPERCONDUCTING POLYMER COATING OF ASSEMBLED DEVICE USING
ELECTRO-DEPOSITION PROCESS**

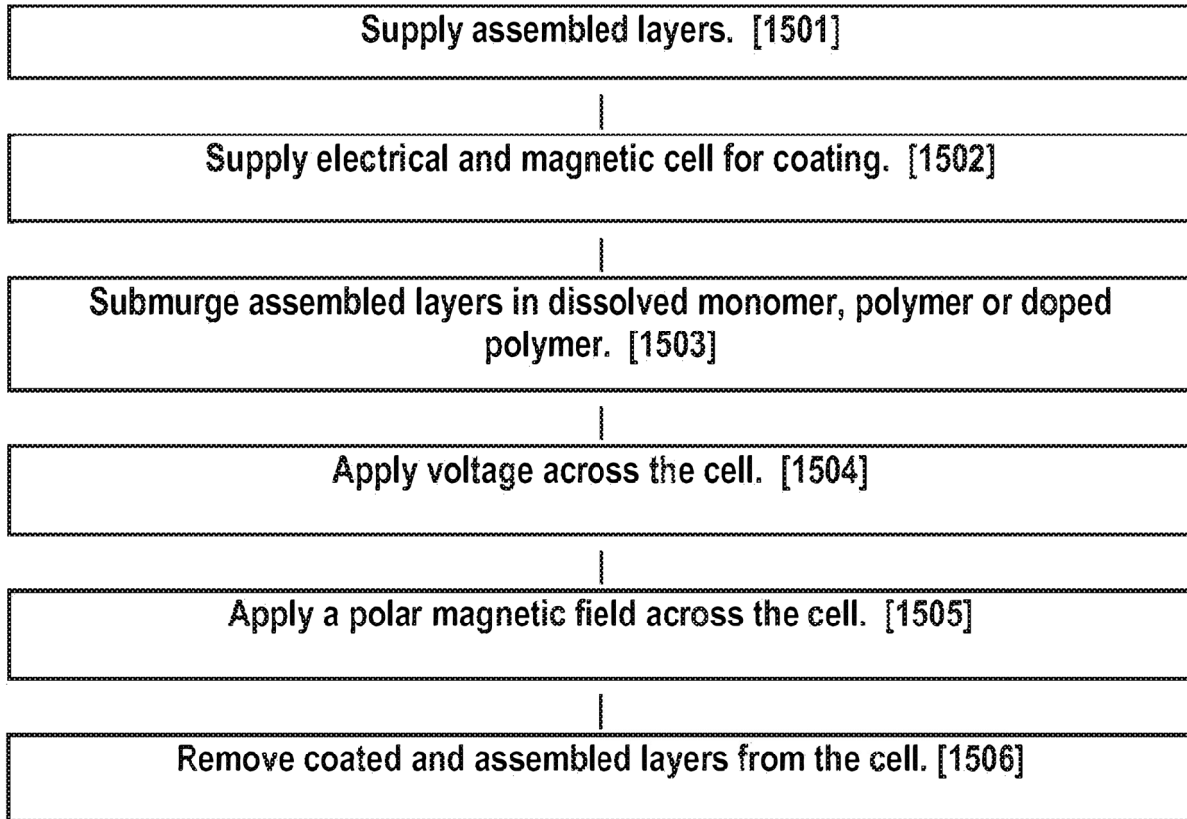


Fig. 21
SUPERCONDUCTING POLYMER COATING OF SEMICONDUCTOR LAYER

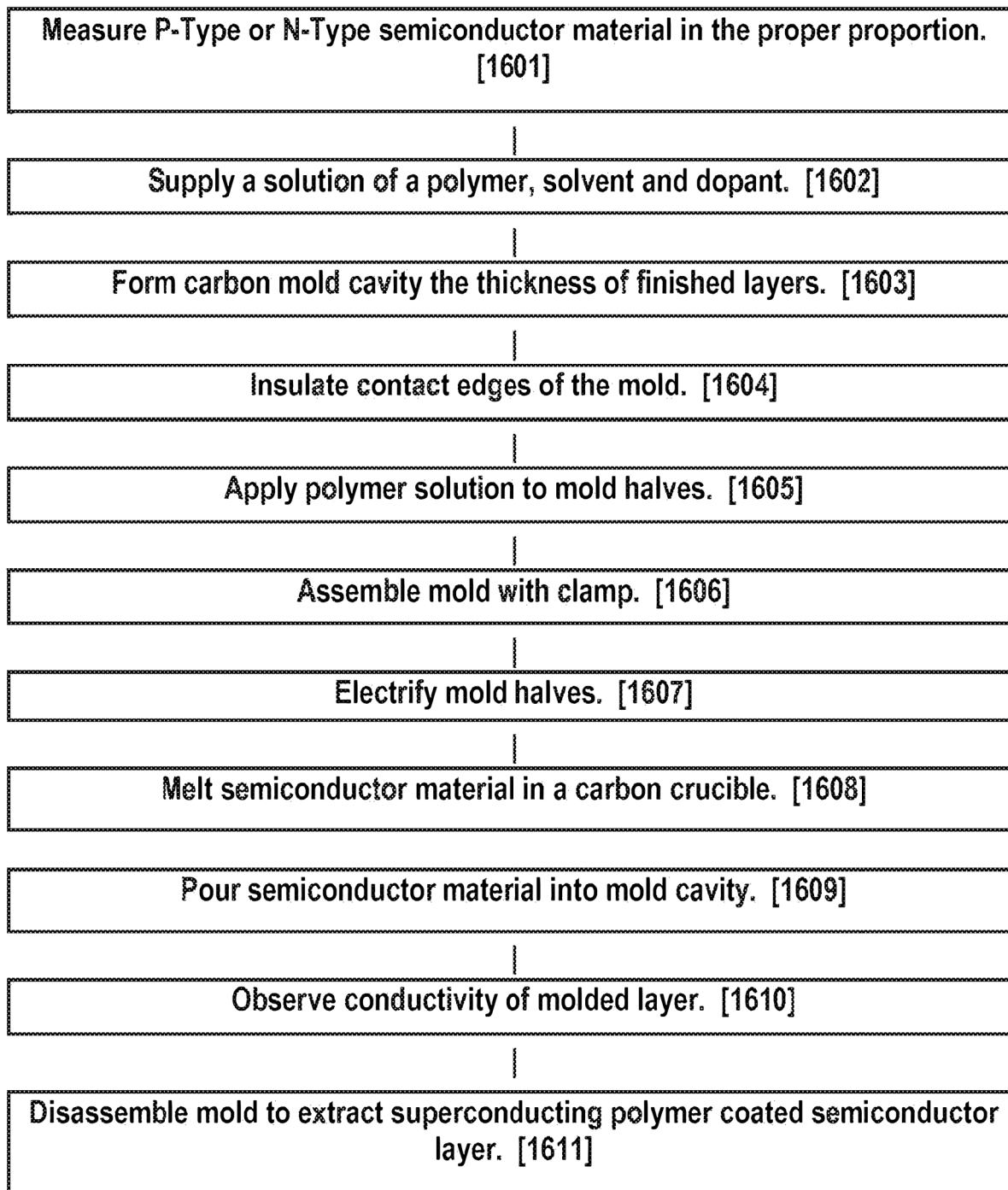


Fig.22

ACTIVATING SUPERCONDUCTIVITY of DOPED POLYMER COATED LAYERS

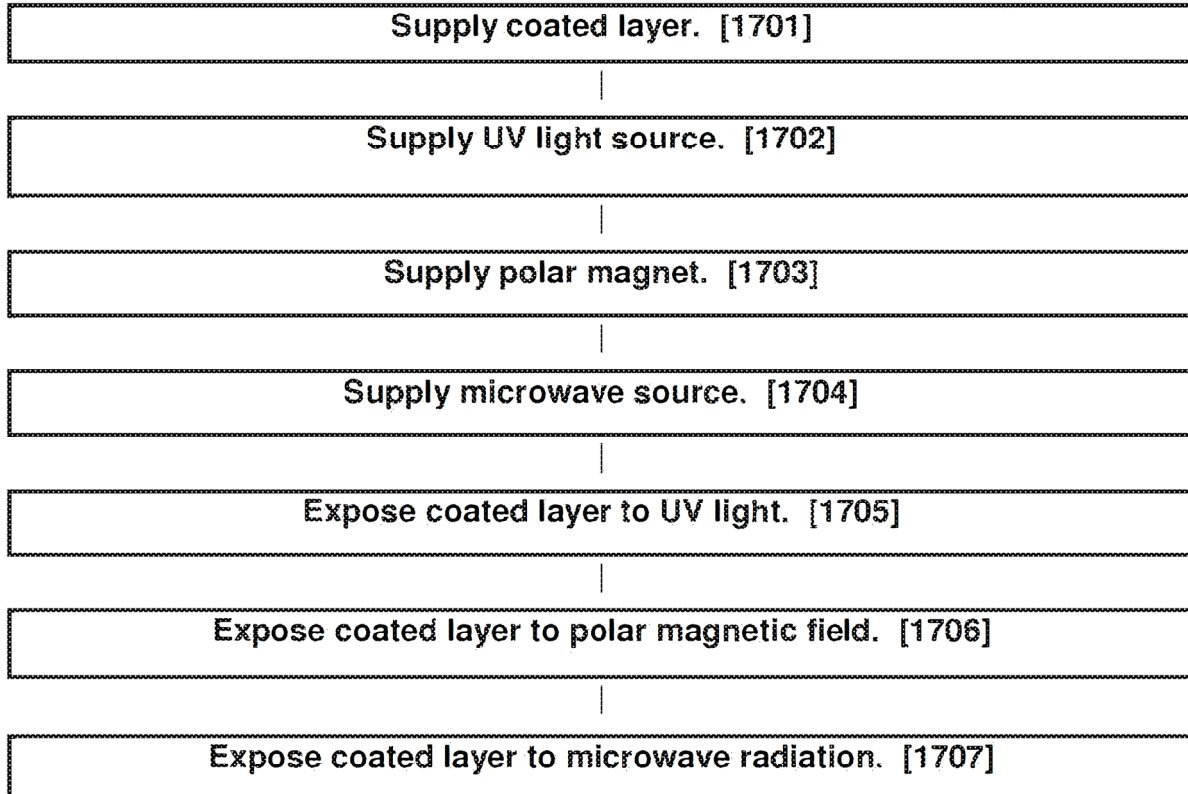
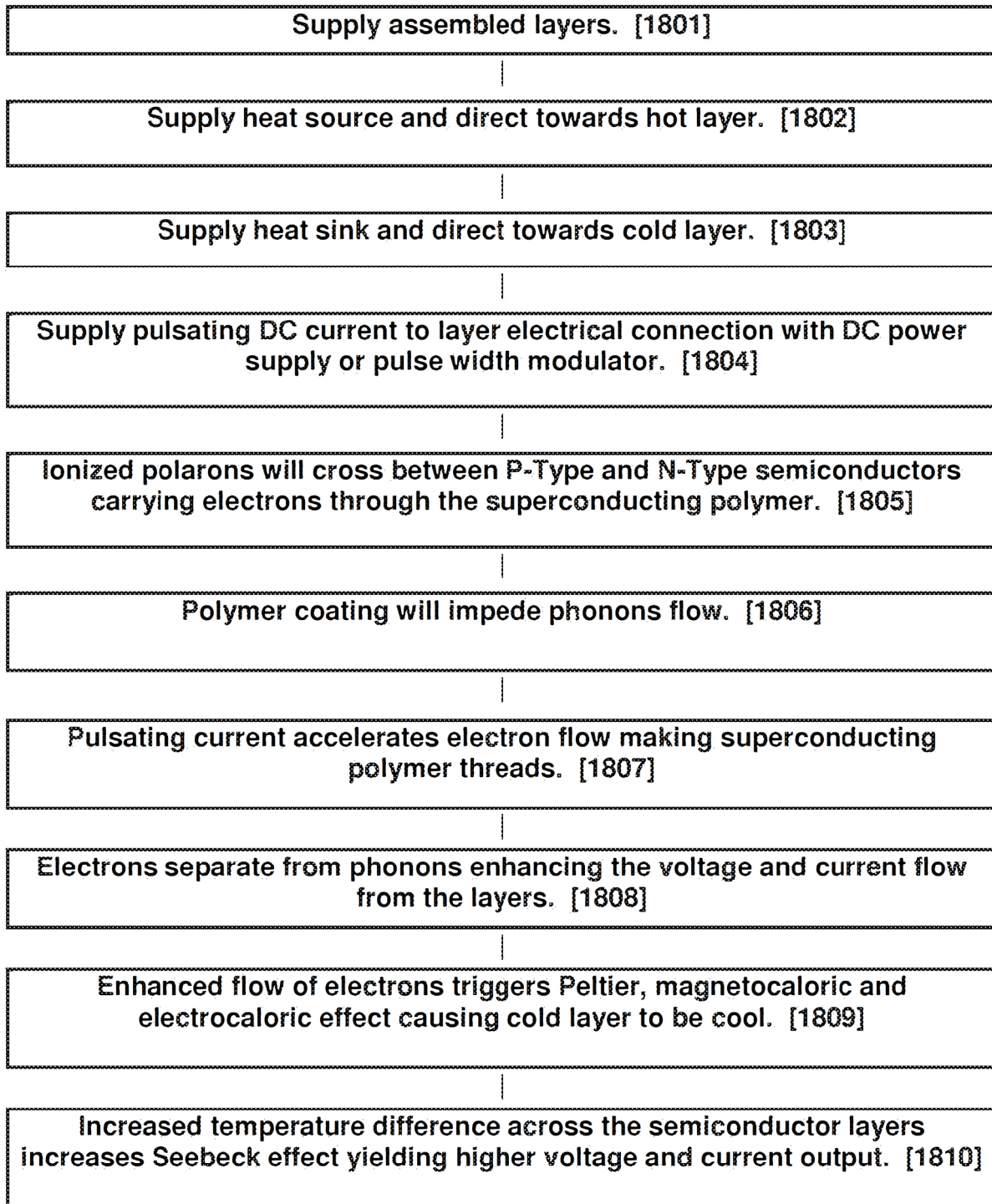


Fig.23
FURTHER ACTIVATING SUPERCONDUCTIVITY of DOPED POLYMER COATED LAYERS



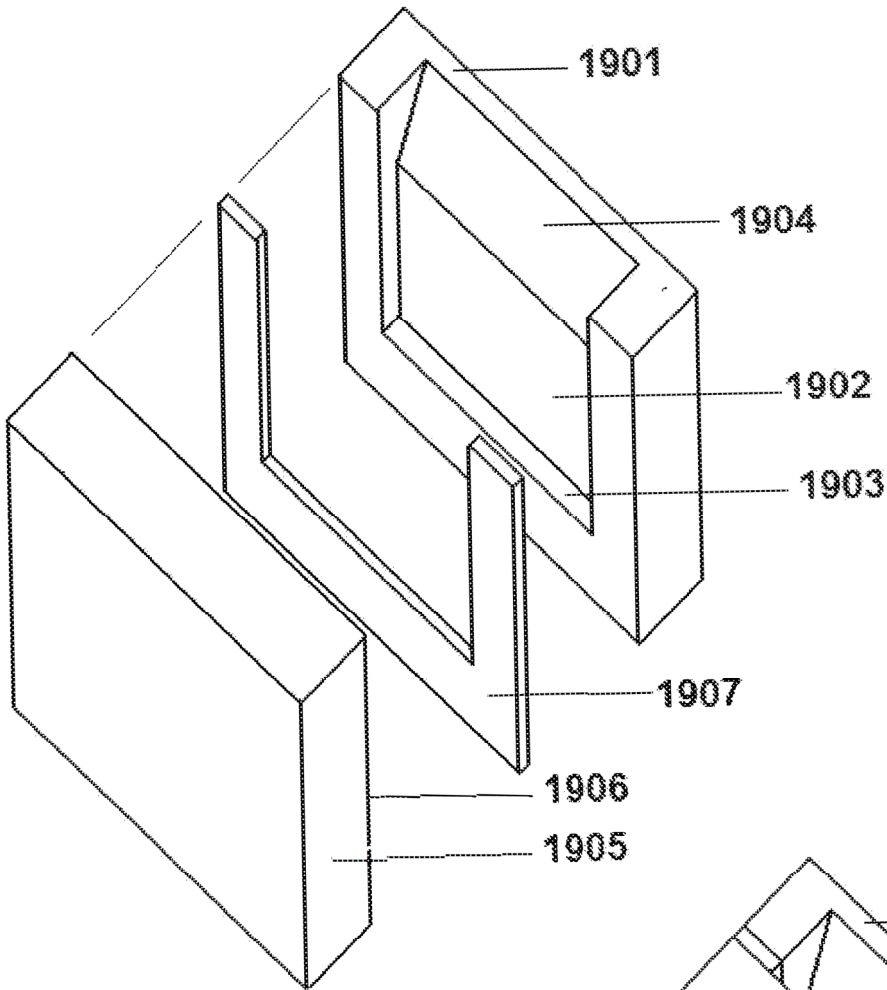


Fig. 24a

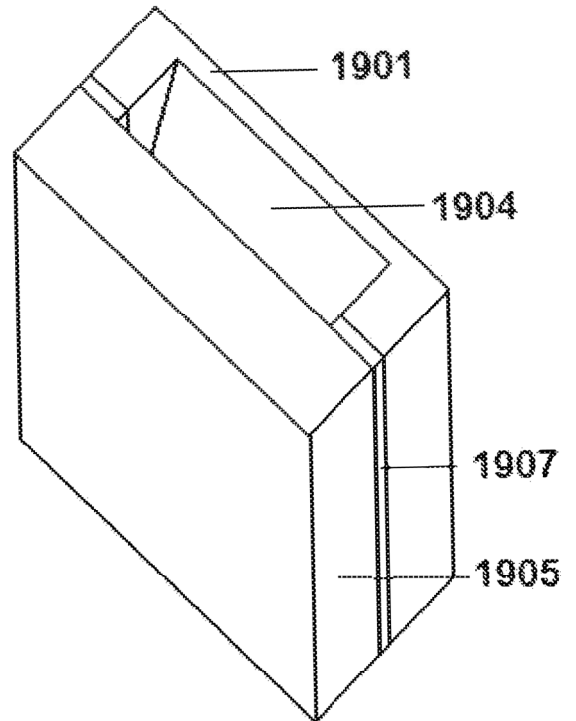
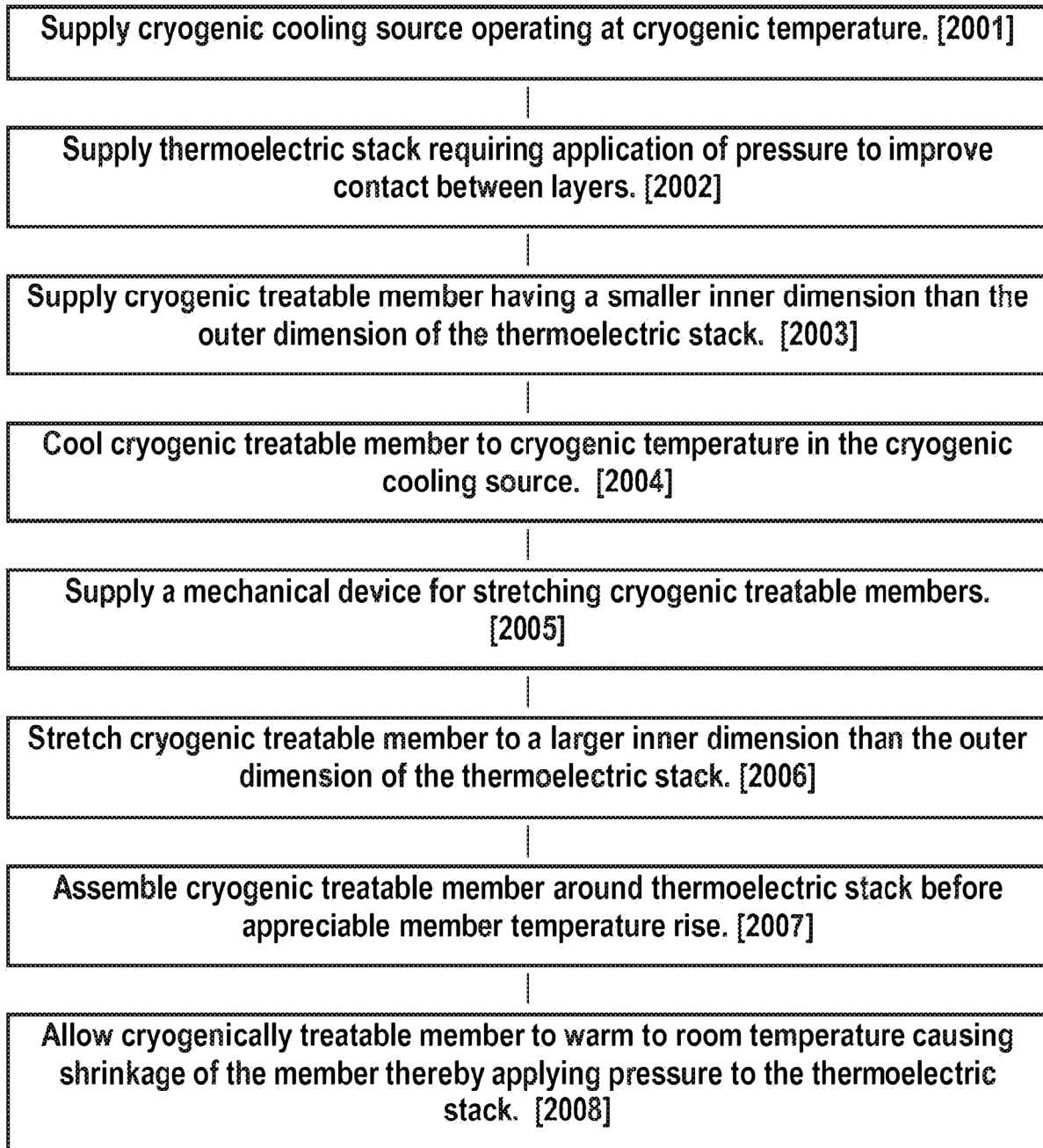


Fig. 24b

Fig. 25
CRYOGENIC MEMBER
INSTALLATION PROCESS



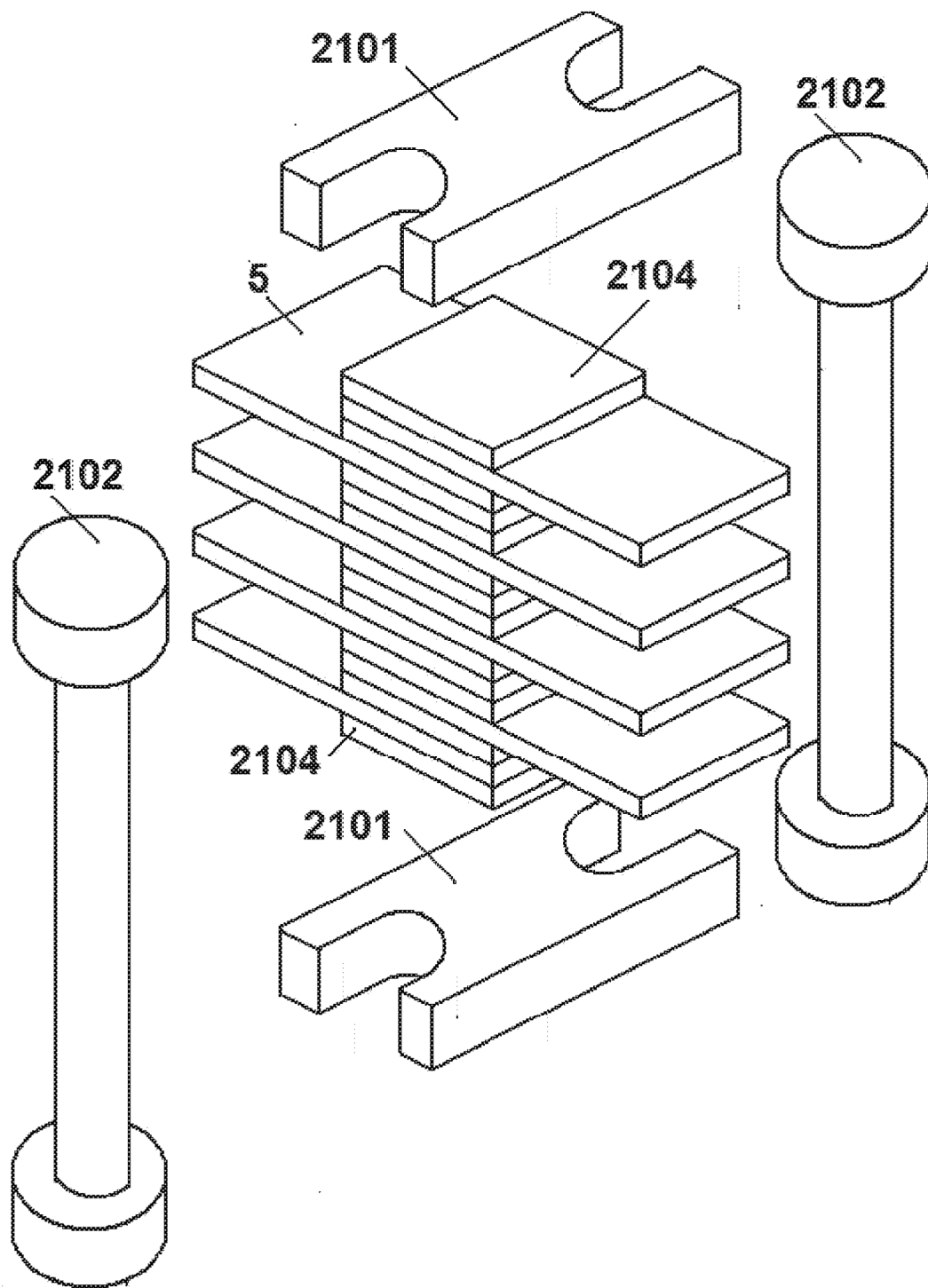


Fig. 26a

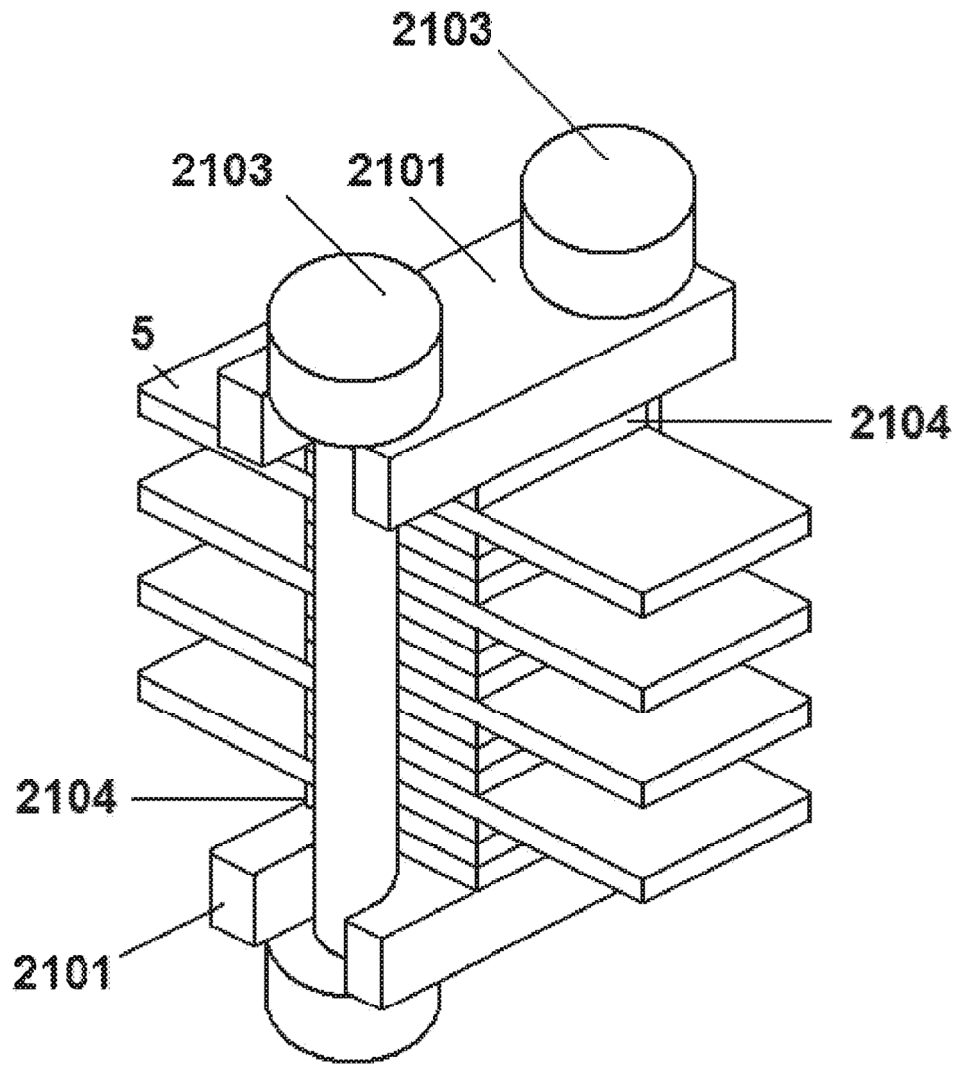


Fig. 26b