DIFFUSION BARRIERS FOR CARBON METAL INTERFACES FOR ELECTRICAL CONNECTIONS, ELECTRONIC AND MICRO CIRCUITRY

BACKGROUND OF THE INVENTION

1. Field of the Invention

One or more embodiments of the invention relates generally to carbon metal interfaces. More particularly, the invention relates to diffusion barriers for interfaces that provide a true metallurgical bond of the device layers with superconducting interfaces and proper thermoelectric properties that are needed for electrical generation devices (Seebeck devices) and cooling devices (Peltier devices), and semiconductor devices, for example.

2. Description of Prior Art and Related Information

The following background information may present examples of specific aspects of the prior art (e.g., without limitation, approaches, facts, or common wisdom) that, while expected to be helpful to further educate the reader as to additional aspects of the prior art, is not to be construed as limiting the present invention, or any embodiments thereof, to anything stated or implied therein or inferred thereupon.

Thermoelectric devices have been developed for various applications requiring temperature differential energy conversion, but these devices face significant challenges in maintaining reliable electrical connections under demanding operating conditions. Traditional thermoelectric device manufacturing relies heavily on low temperature soldering techniques to create electrical connections between thermoelectric elements and metallic contacts. These conventional approaches utilize solder materials that form bonds at relatively low processing temperatures, which inherently limits the operational temperature range of the resulting devices.

Diffusion barrier technologies have been explored to address metal migration issues in semiconductor devices, with various barrier materials being investigated for their effectiveness in preventing unwanted diffusion processes. Conventional diffusion barrier methods in thermoelectric device manufacturing often result in contamination of semiconductor materials with solder metals, which adversely affects the electrical and thermal properties of the thermoelectric elements. The diffusion barrier processes typically introduce metallic impurities into the semiconductor matrix, altering the carefully controlled doping profiles and carrier concentrations that are essential for optimal thermoelectric performance. Furthermore, existing nickel-based diffusion barriers have shown limited effectiveness in preventing metal migration and protecting semiconductor materials from oxidation during high-temperature processing and operation.

Low temperature solder connections create metallic interfaces that introduce unwanted electrical resistance and thermal barriers between P-type and N-type thermoelectric elements. These solder layers form glue-like connections rather than true metallurgical bonds, resulting in junction resistance losses that reduce overall device efficiency. The solder interfaces also interfere with the thermoelectric effects by creating additional metallic layers that disrupt the intended thermal and electrical gradients across the thermoelectric junctions.

The technical problem to be solved involves developing improved diffusion barrier systems for thermoelectric, electronic and microcircuitry devices that can withstand higher operating temperatures while preventing metal contamination and maintaining reliable electrical connections under thermal cycling and mechanical stress conditions.

SUMMARY OF THE INVENTION

In the teachings of this application there are two basic processes to make interconnects for integrated circuits and other non-circuit connections without the use of solders. Details are within the teachings of this application.

Aspects of the present invention provide a fusion-based interconnect method that is more metallurgical and rooted in substrate chemistry. Features of the methods of the present invention include, the following: (1) Low-Temperature Fusion: Operates below 400 °C, and even as low as 200 °C—well within the CMOS thermal budgets. The process uses pressure of 50-100 PSI and low temperature heat to create the fused interconnects. (2) Substrate Engineering: Uses iron iron/nickel plating treated to form iron Martensite crystals, which absorb carbon graphene during heating. This creates a true alloy-like fusion. (3) Solderless Integration: Avoids traditional soldering, solving the issue of graphene’s poor bonding with metals. (4) Ultra-Low Resistance: The electrical resistance of the interconnects is nearly undetectable, boosting speed and thermal efficiency of the circuit. (5) Environmental Edge: Aims to replace copper with graphene, which is safer and more environmentally friendly and sustainable.

The fusion-based process according to embodiments of the present invention can be longer lasting compared to conventional interconnects for several reasons, such as, for example, (1) Metallurgical Bonding: The graphene is fused into a martensitic alloy substrate (iron/nickel), creating a true atomic-level bond. This is more like an alloy than a surface coating, which means it’s less prone to delamination, oxidation, or electromigration. (2) No Solder, No Adhesives: Eliminates weak interfaces that typically degrade over time. (3) Thermal Stability: Martensite structures are known for high hardness and resistance to thermal cycling, which could make the interconnects more resilient under fluctuating chip temperatures. (4) Graphene Fusion Absorption: The graphene isn’t just layered—it’s absorbed into the substrate, which may reduce degradation from environmental exposure or mechanical stress.

A further aspect of the present invention provides for a 2D direct graphene deposition process using chemical synthesis. This process includes (1) Surface-Level Integration: Graphene is deposited on top of the CMOS substrate, which can be more vulnerable, as compared to the fusion process, to delamination or interface breakdown over time. (2) Doping Stability: Intercalation doping improves conductivity, but dopants can diffuse or degrade under heat and electrical stress, potentially reducing performance over time. (3) Standard Substrate: While CMOS-compatible, it lacks the metallurgical robustness of fused martensitic alloy approach.

If it is a priority for maximum durability and minimal degradation over decades of operation, the fusion-based method has the edge. It's more like building graphene into the bones of the chip, rather than painting it on the surface. The 2D Direct Graphene Deposition Process may prove useful, for example, in consumer products, but admittedly, it is not as long lasting as the fusion process. Given the frequency of upgrades to consumer computers, it may work just fine for such devices.

Certain materials may enhance these two processes, including (1) Hexagonal Boron Nitride (h-BN); (2) MXenes (e.g., Ti_3C_2Tx); (3) Transition Metal Dichalcogenides (TMDs) MoS_2, WS_2, and WSe_2; (4) Doped Graphene Variant intercalation doping with atoms like iron chloride, bromine, or lithium; and (5) Amorphous Carbon Allotropes (e.g., Q-carbon).

The fusion methods, according to embodiments of the present invention, could incorporate MXenes or Q-carbon into the substrate alloy for further durability and conductivity. 2D graphene deposition process will evolve into a multi-material layering system, enabling hybrid 2D stacks.

Embodiments of the present invention provide a solderless device can have applications in semiconductor, computing, Peltier and Seebeck devices, for example. As compared to low temperature solders currently used in the art, the bond between layers in the devices of the present invention can withstand higher operating temperatures. Moreover, the fusion methods, as described herein, do not contaminate the solder metals into the semiconductor, as may be the case in conventional methods.

The metal interconnects in devices of the present invention are fused together by a true metallurgical bond of the device layers to provide a superconducting interface and the proper properties needed for semiconductor, Seebeck and Peltier devices.

By impregnating graphene into the semiconductors, oxidation of the semiconductor can be prevented. Graphene acts as a metal diffusion barrier and is a significant improvement over nickel diffusion barriers currently used in the art. In addition, graphene has the ability to self-repair its superconducting web structure and can withstand many thermo cycles during the life operation of devices. Graphene can be used, for example, in a carbonization of martensitic to austenitic structure when impregnated into semiconductors and thermoelectric devices.

Any and all metals that absorb carbon, including phase changing from martensitic to austenitic, while being heat treated, can be used to carbon bond the semiconductors to the phase change metal or material. An electroplated nickel / iron metal is used in the examples discussed herein.

An ideal substrate material is one with low electrical resistance and a good conductor of heat. Copper is used currently in the art as a substrate material in the examples discussed herein, but the substrate can be any metal with similar or equal properties as copper.

The fusion process can use many other substrates other than copper, including any material that bonds to iron / iron nickel plating coatings. If it is needed, the substrate may or may not be electrically conductive. Such would depend on the requirements of the assembly, The iron / iron nickel would still need to be cryo treated, as described below, for the phase changing of iron, but it is the same without the use of copper. Any other material that will bond to iron or iron / nickel can work as the substrate. The entire process could also use pressure and heat, as discussed in greater detail below. Copper may be substituted with these other metals / material in the fusion process depending on the desired effect. Common metals that bond include titanium, platinum, gold, cobalt, palladium, chromium and the like. Other materials suitable for such use include silicon, gallium arsenide, gallium nitride, and the like.

Generally, embodiments of the present invention solve the problem of carrying high electrical currents through a series of interfaces of an electronic device at high and low temperatures with minimal electrical resistance. Embodiments of the present invention also maintain the electrical performance of the electronic semiconductor by impregnating graphene carbon molecules, which bond or fuses with the crystalline structure of the thermoelectric semiconductor, which also acts as a diffusion barrier, protecting the semiconductor from metal contamination and providing a junction that will withstand stresses caused by mechanical bending as well as high temperature gradients.

It is a further objective of the present invention to utilize carbon structures as diffusion barriers that prevent the migration of metals into each other, and also prevent the contamination of the materials in semiconductor devices.

It is a further objective of the present invention to utilize carbon to protect against oxidation of the metals in the thermoelectric and semiconductor devices and other electrical circuits.

The formation of fusion interfaces between the graphene carbon and a metal component is a major breakthrough of the present invention. The metal – graphene carbon fusion requires the metal component to want carbon in its crystalline lattice. This condition exists when a metal that is in the allotropic martensitic state is transformed to the austenitic state. One such metal is class 300 Stainless Steel, for example. This metal can be brought into juxtaposition with the graphene impregnated thermoelectric semiconductor and subsequently transformed from martensitic steel to austenitic steel forming the aforementioned fusion with the carbon that is present after heating. The resulting fusion layer fulfills the requirements for fusing a metal conductor to an active semiconductor with an extremely strong fusion weld without interfering with the semiconductor electrically and providing a temperature and current tolerant superconducting interface. The process can also be improved by drawing the graphene oxide solution into the grain structure of the semiconductor by application of a vacuum before transformation reduction into graphene carbon.

These and other features, aspects and advantages of the present invention will become better understood with reference to the following drawings, description and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Some embodiments of the present invention are illustrated as an example and are not limited by the figures of the accompanying drawings, in which like references may indicate similar elements.

FIG. 1 is a cross-sectional view of a layered structure according to an exemplary embodiment of the present invention;

FIG. 2 is a block diagram illustrating the formation of copper paddles according to an exemplary embodiment of the present invention;

FIG. 3 is a block diagram illustrating the formation of graphene coated semiconductor wafers according to an exemplary embodiment of the present invention;

FIG. 4 is a block diagram illustrating the formation of a thermoelectric device assembly according to an exemplary embodiment of the present invention;

FIG. 5 is a diagram of a three dimensional circuit structure that can benefit from the interconnects according to embodiments of the present invention;

FIG. 6A is a diagrammatic cross section of a thermoelectric stack of the preferred embodiment of the present invention;

Fig. 6B is a diagrammatic cross section of Insert A of Fig 6A including a circuit diagram of the power output circuit;

FIG. 7 is a block diagram of the process for making hot and cold layers from metal bar stock;

FIG. 8 is a block diagram of the process for making hot and cold layers from the powdered metal process;

FIG. 9 is a block diagram of the process for making hot and cold layers with an integral semiconductor layer;

Fig. 10 is a block diagram for making semiconductor layers from the Bridgeman molding process;

FIG. 11 is a block diagram for forming semiconductor layers and concurrent superconducting polymer coating with the direct melting process;

FIG. 12 is a block diagram of the process for making semiconductor layers from the powdered metal process;

FIG. 13 is a block diagram of the process for coating layers using the propylene glycol process;

FIG. 14 is a block diagram of the process for coating layers using the atactic polypropylene process;

FIG. 15 is a block diagram of the superconducting polymer curing process;

FIG. 16 is a block diagram of the process for electric field conditioning of the energy converter assembly;

FIG. 17A and 17B illustration of two alternative switching mechanism modes of operation;

FIG. 18 is a block diagram of the process for coating layers with superconducting paste;

FIG. 19 is a block diagram of the process for using the electro-deposition process for producing coatings of superconducting polymer layers;

FIG. 20 is a block diagram of the process for superconducting polymer coating assembled layers using electro-deposition;

FIG. 21 is a block diagram of the process for coating layers with superconducting polymer during the semiconductor layer formation process;

FIG. 22 is a block diagram of the process of activating the superconductivity of polymer coated layers;

FIG. 23 is a block diagram of the process of further activating the superconductivity in doped polymer coated layers;

FIG. 24A is an exploded view of a carbon block mold;

FIG. 24B is a assembled view of a carbon block mold;

FIG. 26 is a block diagram of the process for installing a cryogenic member;

FIG. 26A is an exploded view of the hardware for installing a cryogenic member; and

FIG. 27B is perspective view of a thermoelectric stack compressed by a cryogenic member.

Unless otherwise indicated illustrations in the figures are not necessarily drawn to scale.

The invention and its various embodiments can now be better understood by turning to the following detailed description wherein illustrated embodiments are described. It is to be expressly understood that the illustrated embodiments are set forth as examples and not by way of limitations on the invention as ultimately defined in the claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS AND BEST MODE OF INVENTION

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well as the singular forms, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one having ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

In describing the invention, it will be understood that a number of techniques and steps are disclosed. Each of these has individual benefit and each can also be used in conjunction with one or more, or in some cases all, of the other disclosed techniques. Accordingly, for the sake of clarity, this description will refrain from repeating every possible combination of the individual steps in an unnecessary fashion. Nevertheless, the specification and claims should be read with the understanding that such combinations are entirely within the scope of the invention and the claims.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details.

The present disclosure is to be considered as an exemplification of the invention, and is not intended to limit the invention to the specific embodiments illustrated by the figures or description below.

As is well known to those skilled in the art, many careful considerations and compromises typically must be made when designing for the optimal configuration of a commercial implementation of any system, and in particular, the embodiments of the present invention. A commercial implementation in accordance with the spirit and teachings of the present invention may be configured according to the needs of the particular application, whereby any aspect(s), feature(s), function(s), result(s), component(s), approach(es), or step(s) of the teachings related to any described embodiment of the present invention may be suitably omitted, included, adapted, mixed and matched, or improved and/or optimized by those skilled in the art, using their average skills and known techniques, to achieve the desired implementation that addresses the needs of the particular application.

There are two parts to build fusion carbon metal interconnects. First are the fusing metals/alloys, typically in the Martensite phase and typically lacking carbon. Second are carbonized materials that have carbon infused. These carbonized materials may be referred to as carbon donating materials. Both parts can be interchanged as the substrate or mounted component, or the parts can form linear interface connections. The finished interfaces, formed as described below, have very low electrical resistance and/or zero interface electrical resistance. The interconnect circuit topography materials and connections are endless and is dependent on circuit design. Many other metals and other materials that form surface bonding, but do not fuse may be used, such as silicon.

Various substrates or component materials can be carbon infused. These materials include carbon, carbon nano-ribbon, graphene, carbon nano tubes, and carbon impregnated metals, ceramics, polymers, sintered metal, powdered metals, alloys, and composites. The materials can be carbonized in any number of processes including grain boundary impregnation, arc plasma deposition, thermo coating processes, electroplating deposition, hydrostatic pressure and/or vacuum impregnation soaking in graphene oxide in deionized (DI) water and reduced to graphene by exposing to electromagnetic radiation and/or any metallurgical process that can either coat or impregnate the materials, including carbon gas impregnation under a vacuum or pressure atmosphere. Also, any and all materials that can be processed to be a carbon donator when interfaced with a carbon absorbing or a phase changing material or metal in the Martensite form can be used.

The carbon absorbing material can be various materials as well. Such materials include carbon absorbing or phase change metals in the Martensite to Austenite phase transition by heating under mechanical pressure. Heating can be done by a furnace, laser welding, laser sintering, hot plates, sono welding, chemical or any other way known in the art. While the description herein may refer to "phase change materials", it is further understood that this term refers to any material that can absorb carbon and produce a bonding or fusion connection with a carbon donating material can be made to work in embodiments of the present invention.

Linear interconnects may be formed from various materials. For example, carbon nano ribbon, graphene, carbon nano tubes and carbon can be joined by heating over lapping carbon materials that have a bonding or phase change material sandwiched between connecting layers. The phase change material is in the Martensite form and can be foil, powdered metals, micro screen, metal compounds that have been reduced to metals and made to be in the Martensite phase. These connecting layers/components can be made by laser sintering printing, electro plating and any way known in the art.

Processes according to embodiments of the present invention can describe methods for making carbon metal interconnects with very low or zero electrical resistance. There are many combinations of substrate and components that can be used in processes to build interfaces and linear connections according to embodiments of the present invention. But there are only two basic material properties that need to be formulated to build fusion interfaces. The first basic material is a metal or metal alloy that can bond or phase change from Martensite to Austenite while being heated. This may be referred to as the metal absorbing member or material of the interface. The metal absorbing material can also be any bonding or phase changing material that absorbs carbon.

The second material for building fusion interfaces is a carbon or carbonized member of the interface. This member may be referred to as the carbon donator.

The carbon donating and metal absorbing properties of the material form the interface that can be made in many different metallurgical processes that is known in the art, from melting and alloying to deposition done by plasma, electrical, arc, impregnation, mixing, wash coating, sintering, printing circuits, micro electronics, chemically, metal compound reduction, annealing and cryogenic treating for phase changing preparation to the Martensite form.

The advantages of this fusion processes are to minimize the use of solders that may contaminate other electrical components by ion metal diffusions and also environmental contamination. The use of graphene in electronics, as described in the example below, referring to the Figures, is a very good metal diffusion barrier and is superconducting. The interface process of embodiments of the present invention forms a true metallurgical fusion of the interfaced components and allows for low or zero electrical resistance of components of carbon for micro electronics and the new quantum circuits in computers.

It should be understood that, with nickel graphene interconnects, the nickel metal does not phase change from Martensite to Austenite, but it is used to prevent oxidation of iron as an alloy of iron nickel. Nickel can be used as a catalyst layer in semiconductor interconnects and becomes the sacrificial metal in the coating bonding of carbon graphene. Nickel is layered on a suitable substrate of silicon or other elements of tungsten, ruthenium or cobalt. A carbon source is layered on top of the nickel, such as graphite or graphene. A mechanical pressure of 100 PSI and heat can be applied to the nickel carbon layer. The carbon defuses through the nickel layer and coats the underlaying substrate in a smooth layer. Many layers can be used by repeating the process. Carbon graphene does not bond with nickel, but it is absorbed through the grain boundaries of the nickel and the excess carbon is deposited under the nickel on the substrate. The sacrificial nickel layer is than removed by etching. Further layers can now be applied to the carbon as desired to make the desired circuit. This process is a bonding of the surface layers and is not a true metallurgical fusion. The bonding has higher electrical resistance than the fusion process and both bonding and fusion processes have their uses depending on the objective.

There are many dopants that can be used in semiconductor interface processes as describes herein. The choice is up to the engineer to use the dopant that is best for the process that is be assembled. Using dopants can alter the final conductivity of a semiconductor interface, so this choice is up to the engineer's designer requirements. There are many dopants used in semiconductors, including but not limited to phosphorus, boron, arsenic, antimony, cobalt, gallium, indium. iron chloride, bromine, lithium, magnesium and aluminum.

The carbon source could also be a dissolved polymer coating on the nickel. Upon high temperature the polymer coating carbonizes and is absorbed though the nickel and also deposited on the substrate. The nickel is removed by etching leaving the carbonized polymer coated on the substrate. The draw back to using the polymer carbonization, is the temperature needed to carbonize the polymer is over the thermos budget for electronic CMOS chips and other electronic components. It should be in the range of 600C to 700C or higher. It could be a good process for other interconnects where a thermos budget is not a problem.

Choosing a process of bonding or fusing is the requirements needed for each process and should be a consideration of the Engineer's objectives and restraints.

One step in creating fusion interfaces is to custom design the process to the best method of forming the connections with the end results clearly in focus, and by selecting a phase change metal or metal alloy that is in the Martensite form ready to absorb carbon from the donator. These metals include iron, iron nickel, stainless steel 300 series, or any metal or material that can absorb carbon and be adapted into a process. The form of the phase change materials can be bulk metal, thin film, powdered metal and powered metal alloys, sintered, electroplated or any other form known in the art. The phase change carbon absorbing material or the metals should be in the ready Martensite form. This can be accomplished, for example, by submerging into liquid nitrogen for 1-24 hours. This cryogenic step changes Austenite phase materials to the Martensite form, ready to absorb carbon.

The carbon donator could be any material that can be impregnated with carbon by alloying, mixing, coating, thermo plasma arc, electroplating, soaking and bushing or any method known in the art. One process, as described in the example below, would be to use graphene oxide to penetrate the grain boundaries using hydrostatic pressure and/or vacuum impregnation, soaking in graphene oxide liquid followed by reducing the graphene oxide by, for example, electromagnetic radiation using any method such as microwaves and/or UV light. If the graphene oxide is deeply embedded into a metal, it may need an electromagnetic spectrum that can penetrate areas thru the thickness of the material, creating graphene from graphene oxide. This additional treatment may be useful, for example, when using porosic sintered metals, sintered copper or similar material with high porosity. Also, other processes can be used, including carbon gas impregnation under vacuum or pressure atmospheres or even simple heat reduction.

In preparing the metallic side of the interface/connector, it is important to be sure the metal, metal alloy or material is in the carbon absorbing phase state. This may be done, for example, with metals, by cleaning then cryogenic treatment by, for example, submerging in liquid nitrogen for 1-24 hours, followed by allowing the metal to gradually return back to room temperature. In this procedure, the metal may be phase changed to the Martensite form and ready to absorb carbon from the carbon donating member of the interface upon heating under mechanical pressure. This cryogenic treatment can be done on bulk metals, metal alloys, sintered metals, powdered metals and may be done after high temperature printer laser sintered deposits for circuits and/or any connecting design topography and methods of metal depositing prior to the fusion step.

The carbon donating material may be any material that is carbon or carbon based composite that donates carbon upon coming in contact with a carbon absorbing metal or material can be used in embodiments of the present invention to make fusion connections. The carbon donating material can be proceeded to contain carbon that can be later donated to a carbon absorbing metal or material.

The process of fusion connections according to embodiments of the present invention can be used for electrical connections as well as for connections other than electrical connections. For example, the fusion connections could be used in place of manufacturing processes that use solders, brazing and welding parts together. The simplicity of the processes according to embodiments of the present invention may be less expensive and easier that other conventional methods for joining and assembling parts. Cost can be reduced by using metals or materials that surface absorb graphene carbon without the cryo-treatment of the fusion process. The downside of this approach may include a higher resistance and a lower lifespan.

The preparation of the carbon absorbing carbon donating parts according to embodiments of the present invention should follow good metallurgical procedures and may be dependent of which materials are used. Examples of some of these processes for the carbon absorbing member of the connection include being sure the metal material is in the form for absorbing carbon from the donating member of the connection. In the case of carbon absorbing metals, this means that they should be in the Martensite phase for the fusion process. Cryogenic treatment in liquid nitrogen is a procedure typically used for assuring the metals are in the Martensite phase. If electroplating or other metal deposition processes are used, the metal should be annealed in a furnace in an inert or reducing atmosphere and, if needed, cryogenic treatments. The process used in preparing the fusion members of the interface may be determined by the design of the device and if the fusion members are carbon absorbing or carbon donating during the fusion step.

It is important when selecting a fusion process for semiconductors that contamination be kept as low as possible to prevent failure of the circuit when building electronic and micro circuits. Each application of the invention may incorporate custom design considerations of the process and the materials being used but is based on two technical scientific principles - one of a carbon absorbing material and one of a carbon donating material during the bonding / fusion process.

While the above primarily discusses using phase changing metals for metal fusion, it should be understood that other metals and / or materials can also bond / fuse to carbon graphene without phase changing.

For example, substrates formed from nickel (10-50%, typically 20-40%, often about 30%) and iron (50-90&, typically 60-80%, often about 70%), either as bulk metal alloys or electro-plated metals, can be used when there are long assembly times and there is a chance for oxidation. Nickel/Iron can be used to prevent oxidation of the substrate prior to fusing.

When using nickel, it has been found that this is not a true fusion to the substrate, but is only a bond with the graphene carbon. The graphene carbon only penetrates between the grain boundaries of the nickel crystals and is not a true alloy of nickel graphene carbon. Further, nickel substrates use for electrical interconnects do not allow for the lowest electrical resistance, as the nickel bond does not share electrons with the graphene carbon. Further, nickel absorption of graphene carbon is a mechanical absorption within the grain boundaries of the nickel. similar to a sponge absorbing water. Pure nickel, it has been found, does not heat treat without being alloyed with other heat treatable elements for carburizing. Accordingly, electronic interfaces using graphene carbon bonded nickel is a poor interface, as the operation of the electronic circuit that produces heating and cooling over time will push out the graphene carbon from the nickel interface and result in failure of the circuit as used in metallurgical decarbonization of nickel.

It has been discovered that nickel graphene carbon used in interface bonding, then etched to remove the nickel, must have a graphene carbon absorbing underlay, such as Martensite iron or other graphene carbon absorbing metal or material or the circuit will fail.

To that end, it has been found that iron graphene carbon fused interfaces are long lasting, forming a true metallurgical fusion as the fusing creates an alloy of the iron with the graphene carbon, sharing electrons. Iron graphene carbon fused circuit interfaces used in electronic micro circuits can have undetectable electrical resistance within the interface. The electrical resistance of iron graphene carbon fusion is that of the substrate’s metal or material of the interface. The electrical resistance of the iron graphene carbon fused interface is a ballistic conduction of the substrates.

Accordingly, iron graphene carbon fused interfaces within integrated circuits allows for faster computers and electrical circuits. The iron graphene carbon fused interfaces disperse heat generated within the circuit, allowing for low operating electronic temperatures. Further, the iron graphene carbon fused interfaces is a diffusion barrier for metal migrations and oxidation.

While the above refers to iron or iron / nickel alloys, it has been found that any metal or material that can fuse to graphene carbon can be used for interfaces in electrical circuits.

The iron graphene carbon fused interconnects can be used for various purposes. In addition to uses in electronics, uses can include soldering, brazing, welding and connecting materials together using the same parameters as described herein. The iron graphene carbon fused circuits can replace copper and can be environmentally safer than other metals used in various processes, such as in solders.

A specific application of the present invention is described below, where a thermoelectric device is formed using the fusion connections according to embodiments of the present invention.

Referring now to FIGS. 1 and 2, copper paddles can be prepared. Copper is typically used as the substrate for the hot and cold paddles because of its high conductivity and low electrical resistance, typically on the order of $1x10^{-7}$ to $1x10^{-8}$, for example. It should be noted that copper is usually a contaminate of bismuth-tellurium semiconductors.

According to an embodiment of the present invention, a copper substrate 11, 13 can be cleaned and prepared for electroplating. Various metals can be used for electroplating onto the copper substrate. In this embodiment, in step 200, a nickel / iron (40/60) solution can be used in an electroplating tank to form an electroplating 41 onto the copper substrate 11, 13. It should be noted that nickel and iron is not a contaminate of bismuth-tellurium semiconductors.

Typically, the electroplating can take place for about 3 minutes and, when complete, the electroplated copper substrate can be removed from the tank, rinsed and dried.

The nickel iron content in the plating bath may vary according to application. In some embodiments, a 40% nickel / 60% iron alloy may be used. In some embodiments, the maximum nickel content may be about 40% as the nickel/iron alloy may be used to prevent oxidation of the iron in the interface if occurring before and after fusion of the interface. Typically, it is desirable to use the lowest nickel content in any of the processes because the fusion occurs with the iron that is in the alloy and not the nickel, for the most part. Often, it is desirable to use the lowest nickel content possible to still prevent oxidation of the interface after fusion and in operation of the units. If there is no concern of oxidation before or after the fusion process, then iron alone could work, either electroplated or in powder form where needed. If only iron is used, the parts should be protected from oxidation after the cryogenic treatment until the fusion assembly is completed. In some embodiment, the graphene that is fused to the iron in the interface could protect the iron in the now fused joint, as the graphene may protect the iron from oxidation / diffusion.

In step 210, the electroplated copper is annealed to bond the electroplated metal to the copper substrate. In some embodiments, the electroplated copper can be put in a quartz lined tube furnace and annealed for 3 hours at 600C in a hydrogen atmosphere. The furnace is then allowed to cool to room temperature while under a hydrogen or argon atmosphere.

Depending on the specific material, Martensite phase material may start to transform to Austenite at approximately 230C and above. Typically, below 230C there is no transformation occurring. Above 230C, the transformation speed may be determined by time and temperature. A lower temperature may be suitable for use in surface mounting of circuit board components as well as any heat sink components in electronic/electrical applications. Micro electronic circuits can be processed with the use of precision laser and sonic micro heating. The lower transformation temperature can replace solders that are used at the same temperatures but giving a low electrical resistance fusion joining. The benefit of the fusion process of the present invention over low temperature solders is what occurs with solder components that reach re-melt temperatures in over heated electronic circuits. By using the fusion process of the present invention, the joint can become stronger if the electronic circuit becomes over heated because the Martensite remaining would continue to transform to Austenite, strengthening the fusion joint.

The electroplated copper is removed from the room temperature furnace and immediately put into liquid nitrogen, typically for about 6 hours, to change the electroplated metal (in this case, the electroplated nickel / iron) from austenitic phase to the martensitic phase in step 220. Finally, in step 230, the electroplated copper is stored under vacuum, such as in vacuum bags, until assembly.

The transformation from Austenitic to Martensite phase may occur instantly at cryogenic temperatures. This feature may also be good for circuit board processing, where automation assembly time is limited. Using micro cryosurgery, dermatology type devices can be used for production of circuit boards or micro repairs. Also, the annealing step after electro plating of the iron alloy on the substrate can be combined in one step during the fusion heating process if desired.

Referring to FIGS. 1 and 3, thermoelectric semiconductor wafers 12, 14 can be, for example, bismuth-tellurium semiconductors. The thermoelectric semiconductor wafers 12, 14 (also referred to as semiconductors 12, 14 or wafers 12, 14) can be made by various methods, such as the Bridgeman method of crystal growing. Once grown, in step 300, the semiconductor wafers 12, 14 can be cut to the desired size.

In step 310, the semiconductor wafers can be annealed, such as in a hydrogen gas quartz tube at 300-400C for 3 hours. The annealed wafers are allowed to cool under hydrogen or argon atmosphere to room temperature.

The semiconductor wafers are removed from the annealing furnace and immediately submerged in a solution of distilled water and graphene oxide, in step 320. The graphene oxide may be present at a concentration of 0.01% for example. The solution with the wafers may be placed under a slight vacuum below the vapor pressure of the solution and / or may be placed in a high pressure chamber for 5 hours. This vacuum or pressure can help impregnate the wafer grain boundaries and surface with graphene oxide.

The wafers are then removed from the solution and dried, in step 330, in a chamber of argon at about 50C for 2 hours. In step 340, the semiconductor wafers are then removed from the drying chamber and are treated with a reducing agent, such as electromagnetic radiation for 15 seconds, to reduce the graphene oxide to graphene.

It should be understood that, after treating the semiconductor with graphene oxide and reducing it to graphene, the semiconductor fracture/brake properties become much stronger as compared to the original wafer. This can be very beneficial to working with bismuth/tellurium thermoelectric wafers because the untreated wafers are very fragile and brake quickly upon uneven pressure.

In step 350, the semiconductor wafers are lightly sanded on their four sides to remove surface graphene, leaving surface graphene 42 on the two flat interface surfaces. The semiconductor wafers 12, 14 are now ready for assembly.

Referring now to FIGS. 1 and 4, a thermoelectric device assembly 10 can be assembled as described herein. In step 400, the first copper electroplated nickel/iron plated substrate 11 can be layered with a first p-type semiconductor wafer 12, then another copper substrate 13 and then an n-type semiconductor wafer 14. This makes up one full element of a thermoelectric Seebeck or Peltier device, for example.

In step 410, the thermoelectric device assembly 10 can be clamped together under high pressure with the use of a clamp or a cryogenic treat shape memory alloy that applies pressure in the heating fusion step of the assembly, described below. The clamp or shape memory allow can be insulated from the elements by, for example, a high temperature mica inserted between the clamp and/or shape memory alloy. While FIG. 1 shows a particular cross-section, the device assembly 10 can be made up of many elements and could be in any shape or configuration, such as linear or circular.

In step 420, the entire assembly 10 can be put into a quartz furnace and heated to below the melting temperature of the bismuth-tellurium semiconductors (440-500C) and held at this temperature for 3-10 hours, with the exact time being determined by trial and error and the desired fusion bond. In step 430, the assembly is then slowly cooled to room temperature and removed from the furnace.

While being heated, the shape memory alloy can shrink, applying pressure to the entire assembly, for example. The fusion bonding takes place in what is known in the heat treating industry as the carbonization of the martensitic to austenitic phase change as the metal absorbs the carbon impregnated semiconductor.

What is normally considered a cold junction of the interfaces of the semiconductor with the copper substrate is now a fusion bond of the semiconductor, nickel/iron and copper. This fusion bond is required for operating a Seebeck thermoelectric device, for example.

The semiconductor junctions formed by the methods of the present invention now super conduct into the copper and the total resistance of the device has the resistance of copper with no loss due to the junctions. In other words, the device total resistance is that of one piece of copper. The electrical conduction is both top-down and bottom-up conduction using a pulse width modulator switching power supply.

The use of conventional low temperature solders is suitable for Peltier devices, but fall far short of operation in high temperature devices because the low temperature solders of today are not considered fusion bonded, but are, in fact, metallic glues that have good electrical conduction suitable for Peltier devices, but not a fusion bonding requirement that is needed for good bimetal thermoelectric Seebeck devices.

FIG. 5 illustrates packaging for a three-dimensional circuit, where package balls, bumps and micro bumps are used to build a three-dimensional circuit. FIG. 5 is just one example of such a circuit, and it should be understood that aspects of the present invention can be applied to various other circuits, including quantum computing circuits, via interconnects, and the like. The interconnect provided by the balls, bumps pillars, and micro bumps may be provided via graphene carbon fused interconnects, as described above.

In such 3D integrated circuits (3D ICs), the processes of the present invention may be used in hybrid bonding and interconnect technology for logic, memory, sensors chips and the like. Further, bonding, using the fusion process according to embodiments of the present invention, within the thermo budget of the chips and the graphene surface layer bonding with chemical dopants can be used to form vertical interconnect stacks. Such processes can reduce wire connections, where shorter interconnects conserve power and disperse heat using graphene, enhances bonding strength, reduces contact resistance at the interface, provides a smaller footprint, prevents metal diffusion contamination, provides a simpler process with lower manufacturing cost over other processes, provides backside power delivery, can be in parallel connections or in series for transistors and in parallel for multi transistors, can be used in CMOS Logic NMOS and PMOS to reduce power consumption, provides die to die connections, replacing Cu-Cu bonding with the graphene fusion process or surface graphene bonding using chemical dopants with both using pressure and heat.

These entire processes are designed to eliminate or reduce copper use, replacing copper with graphene using the two graphene processes, as described herein, with pressure and heating to fuse or bond the interfaces of the circuit.

There are many different ways and materials used to incorporate graphene in integrated circuits. The final design is the decision of the engineer and the desired objective result.

The processes described above, using the fusion process and / or surface bonding of layered doped graphene, may be useful in transistor manufacturing. Both graphene processes play a role in building graphene-based transistors. Such processes can provide the following features: (1) It enables low temperature metallurgical bonding as low as 200C; (2) Interconnects between transistors; (3) Graphene interconnects in GFETs (Graphene Field Effect Transistors) interconnects to link the source, drain, and gate terminals; (4) Fuse graphene interconnects to the metal contacts, reducing resistance and improving thermal performance; (5) Packaging and assembly fusion method in the final packaging stage. Bonding graphene-based chips to the substrates without degrading their properties which can be valuable for flexible electronics using low temperature bonding; (6) Thermal Management. Graphene’s exceptional thermal conductivity combined with the fusion process, described herein, dissipate heat from densely packed transistors arrays; (7) Semiconducting graphene channels with dopants used to create bandgap switching for logic transistors. Dopants used can be Boron (B), which induces P-Type Electron deficiency and Nitrogen (N), which induces N-Type behavior as extra electrons, into the Graphene lattice. Breaks graphene symmetry and alter its electronic structure creating Bandgaps; (8) Other Dopants used, including oxygen group and metallic dopants; and (9) Other bandgap methods using nanoribbons and bilayer twisting can also be used.

Fig. 6a and 6b, shows a cross sectional view of a single module (A) of the present invention assembled between multiple modules of the preferred embodiment of the present invention that operates as thermoelectric generator by converting heat energy into electrical energy. The basic principle of operation of the thermoelectric generator is that heat from heat source 101 travels through hot layer 107 to semiconductor layers 110 and 108 where the thermal energy is converted into electrical energy. Cold layers 109 and 111 conduct any excess heat to the heat sink 102 where the heat is discarded.

The components of the preferred embodiment of the present invention are a heat source 101 which is forced air, but may be any solid, liquid or gas at an elevated temperature, a heat sink 102 which is also forced air, but may be any solid, liquid or gas at equal or lower temperature than the temperature of the heat source 101. An electrical load 103 of Fig. 6b, is connected electrically to the thermoelectric stack 105 by electrical conductors 104. The preferred embodiment is explained as using a stack of thin layers having a flat planar relationship to each other however the spirit of the invention extends to any physical size and shape of the thermoelectric and heat carrying elements including but not limited to toroidal and tubular. A switching mechanism 106 further connects the electrical load 103 to stack 105.

The stack 105 is made up of layers as shown in (A) and consists of a sintered copper layer 107 for conducting heat from the heat source 101 to the P-Type semiconductor layer 108 and N-Type semiconductor layer 110 for converting heat energy to electrical energy, a sintered copper layer 109 for conducting excess heat from layer 108 to the heat sink 102 and also conducts electrical energy from the stack 105 to the load 103. In addition a N-Type semiconductor layer 110 for converting heat energy to electrical energy, and a sintered copper layer 111 for conducting excess heat from layer 110 to the heat sink 102 and also conducts electrical energy from the stack 105 to the load 103.

All of the layers of the stack 105 are coated with a superconducting polymer for carrying electrons (un-shown) and impeding the flow of phonons (un-shown) through superconducting polymer threads (un-shown) to adjoining sintered copper layers 107, 109 or 111, or P-Type semiconductor layer 108, or N-Type semiconductor layer 110. A cryogenically applied metallic member applies 5,000 - 30,000 PSI pressure to the top and bottom of the stack at Insert A to insure good thermal and electrical contact throughout the stack 109, 108, 107, 110, 111 of Insert A.

Fig. 6b shows a sectional view of a single module (Insert A) assembled in the electrical circuit of the preferred embodiment of the present invention. The switching mechanism 106 connects load 103 across the stack 105. The switching mechanism 106 connects the load through two electrical paths 112 and 113 typically to convert the direct current output from the stack 105 to an alternating current 103. An important feature of the preferred embodiment of the present invention is that the electrical path 113 be established before the electrical path 112 is severed as illustrated in Fig. 17a. An alternative embodiment having a quiescent period between the breaking of first path 112 and establishment of a second path 113 is illustrated in Fig. 17b.

Hot layer 107 as well as cold layers 109 and 111 are made of materials that are good conductors of heat and electricity. The material for making hot and cold layers of the preferred embodiment of the present invention is, but is not limited to, copper. Block diagrams of process steps for forming the hot and cold layers of the preferred embodiment of the present invention are found in but not limited to Fig. 7, Fig. 8 and Fig. 9. The process of Fig. 9 forms semiconductor layers that are integral with the hot and cold layers. Other combinations of materials and processes that can be utilized but are not limited to in the formation of hot and cold layers include electrically conducting, semi-conducting and non-conducting materials, thermally conducting, refractory or insulating materials or materials having physical properties of solid, crystaline, lattice structure, amorphous, non-porous, granular, micro-particulate, nano-particulate, porous metal and non-metal structures and are bound together by sintering, cohesive bonds, adhesive bonds, cementitious materials, polymers and epoxies and anyone or any combination of the aforementioned materials or processes.

The cold layers 109 and 111 as well as the hot layer 107 are optionally coated with a diffusion barrier to prevent metal ions from migrating into the adjoining layers. The ion diffusion barrier coating of the present invention is a form of carbon, such as graphene, that can be applied with any of the processes well known in the art. The graphene may be directly applied or may be formed in situ, as described herein. The graphene diffusion barrier may also help dissipate heat from the product.

Layer 108 of the preferred embodiment of the present invention is a N-Type semiconductor. The materials for making the N-Type semiconductors for the preferred embodiment of the present invention are but are not limited to Bismuth-Tellurium-Selenium, or any N-Type thermoelectric semiconductor material known in the art.

Layer 110 of the preferred embodiment of the present invention is a P-Type semiconductor. The materials for making the p-type semiconductor are Bismuth-Tellurium-Selenium and Antimony or any P-Type thermoelectric semiconductor material known in the art.

Other combinations of materials and processes that can be utilized but are not limited to in the formation of N-Type or P-Type layers may include electrically conducting, semi-conducting and non-conducting materials, thermally conducting or low thermally conducting, refractory or insulating materials or materials having physical properties of solid, crystalline, lattice structure, non-porous, granular, micro-particulate, nano-particulate and porous structures and are bound together by sintering, cohesive bonds, adhesive bonds, cementitious materials, polymers, metals, epoxies and anyone or any combination of the aforementioned materials or processes.

All of the layers 107, 108, 109, 110 and 111 are coated with a conductive hydrocarbon typically in the form of a superconducting polymer to enhance electrical conductivity through superconducting polymer threads. The specific coatings of the preferred embodiment of the present invention are but not limited to propylene glycol derivatives applied using the method steps but not limited to the process steps of Fig. 13 or atactic polypropylene applied using the method steps but not limited to the process steps of Fig. 14 in either case followed by the conductive polymer coating curing process but not limited to the process steps of Fig. 15.

The major breakthroughs of the preferred embodiment of the present invention solve the inherent engineering problems of thermoelectric devices.

The first breakthrough of the preferred embodiment is achieving a superconducting polymer coating on the P-Type and N-Type semiconductor layers 108 and 110 without oxidation of the semiconductor materials. This is accomplished by use of the process of Figs. 11 and 21 that forms superconducting polymer threads as the semiconductor material is cooling in the mold. The disadvantage of this process is that any finishing of the cast semiconductor layers after casting will remove the superconducting polymer and promote oxidation of the semiconductor material. The semiconductor layer shrinks unevenly in the mold creating irregularities that are not conducive to intimate contact with adjoining layers in a stack 105. The preferred embodiment of the present invention therefore uses the cast semiconductor layers in the as cast condition and builds up the thickness of the superconducting polymer to form long superconducting polymer threads using the processes of Fig. 21 to a thickness greater than the dimension of the as cast surface irregularities.

Subsequent processing the surface of the superconducting polymer through thermal deformation is used to promote intimate contact between thickly coated adjacent layers in the stack 105.

The second breakthrough of the preferred embodiment of the present invention is in reaction to the thermal expansion of the electro thermal components of the stack 105. The Copper hot layers 107 could expand as much as 80 microns when heated 121 degrees Celsius by the heat source 101.

Assuming that the heat sink 102 remains at ambient temperature the cold layers 109 and 111 do not expand. Therefore the two superconducting polymer layers between layer 107 and 108 could be exposed to a relative shift of 40 microns.

The present invention depends on the thickness of the superconducting layers and the resilient properties of the strong attractive ionic bonds of superconducting polymers under electric load, to maintain superconducting polymer threads while undergoing the sheer stress due to thermal expansion.

The third breakthrough of the preferred embodiment of the present invention is to replace the cohesive bonding that is expected from the solders used in the prior art as well as the spring biased band of the toroidal prior art thermoelectric devices. The preferred embodiment of the present invention utilizes a resilient member having a single component that generates the holding force as well as applying the force equally to all layers. The material of the resilient member is conditioned under cryogenic temperature, expanding the original shape. The resilient member is assembled over the stack 105 and allowed to warm to room temperature. As the resilient member warms it contracts and applies an evenly distributed force to all layers of the stack 105 especially in a toroidal thermoelectric generator or any appropriate configuration.

The fourth breakthrough of the preferred embodiment of the present invention allows the conversion of heat into electrical energy at high temperatures. The polymers that are coated and made superconducting per the inventive processes at Figs. 13, 14, 15, and 19-23 continue to be superconducting after being carbonized. Such polymers form graphene under the conditions of the present invention. Accordingly, the present disclosure provides a method for the production of graphene as well as the providing graphene with the electromechanical properties described herein.

The fifth breakthrough of the preferred embodiment of the present invention is a cooling effect of the cold thermo conductive layers during the conversion of heat to electrical energy. This effect shows that the inventive thermoelectric process herein described produce a device that will operate at a higher efficiency than can be explained exclusively by the temperature difference between the heat source and the heat sink.

These breakthroughs have resulted in the discovery of a method of producing pristine graphene that uses conductive polymers that may be treated at high temperatures. The polymers may be disposed a in tightly packed plastic filled reaction chamber. The electrically insulated vessel is energized with electrodes with high electrical current conducting through the polymer and plastic. The process produces high temperatures, reducing the polymer and plastic to high quality, pure, pristine graphene that has properties including the ability to super conduct electricity. Such graphene can be used in electrical and electronic applications and as reinforcing additives in steel, alloys, plastic and composite materials, concrete, and the like. Dopants can be added to make specialized Graphene for customized applications. In some embodiments, the plastic and polymer can be coated with something electrically conductive, using superconducting plastic or could be plastic with dopant that is the conductive source, such as coal ash, for example. In some embodiments, dirty plastic, such as that from a circuit board, can be used that may be contaminated with metals, for example, where the metals can be recovered through volatilization of the metals to purify the graphene even further.

Fig. 7 is a block diagram of the process for making thermal conductor hot and cold layers out of metal bar stock of the present invention. In process step 201 the bar stock is cut to the appropriate size for the hot and cold layers. In process step 202 the layers are coated per the atactic polypropylene process of Fig. 14 or the propylene glycol - coating processes of Fig. 13. This is followed by process step 203 calling for curing the coating using the superconducting polymer curing process of Fig. 15.

Fig. 8 is the process for making hot and cold layers for the preferred embodiment of the present invention using the powder metal process of sintering. In process step 301, hot and cold layers are formed under pressure into appropriate size and density of 88-98% using copper powder in the micro to nanometer size range. This is followed by process step 302 where the formed hot and cold layers are sintered and annealed in a reducing atmosphere near the melting temperature of copper. The next process step 303 calls for coating the sintered and annealed hot and cold layers using the atactic polypropylene process of Fig. 14 or the propylene glycol coating processes of Fig. 13. The final process step 304 cures the coating using superconducting polymer curing process of Fig. 15.

Fig. 9 is a block diagram for the process to make hot and cold layers with an integral semiconductor layer. Process step 401 requires a supply of formed layers from the metal bar stock process of Fig. 7 or the powdered metal process of Fig. 8. This is followed by process step 402a where a layer of N-Type or P-Type semiconductor material is deposited on the metal layer using but not limited to electroplating, vapor deposition, vacuum deposition, plasma sputtering processes. Alternatively a composite 402b of P-Type and N-Type particles suspended in a polymer can be applied by any appropriate process. The resulting part is then coated in step 403 using atactic polypropylene coating process of Fig. 14 or the propylene glycol coating processes of Fig. 13. Lastly process step 404 the coating is cured using the superconducting polymer curing process of Fig. 15.

Fig. 10 is a block diagram for semiconductor layer formation using the Bridgeman molding process. The first process step 500 calls for measuring P-Type or N-Type semiconductor material in the proper proportion. At step 501 the P-Type or N-Type semiconductor materials thoroughly mixed. Melting of the P-Type or N-Type semiconductor mixture commences at step 502. In step 503 the mixture is cooled slowly to form a thermoelectric ingot followed by slicing the ingot into layers of appropriate size at step 504. Step 505 calls for lapping, grinding or polishing the slices of the ingot. At step 506 the layers are annealed in a reducing atmosphere. Annealing is followed by an optional coating process 507, of each layer with metal ion diffusion barrier which is done with graphene. Step 508 calls for coating the semiconductor layer using the atactic polypropylene process of Fig. 14 or the propylene glycol coating processes of Fig. 13. The last step 509 is curing the coating using the superconducting polymer curing process of Fig. 15.

Fig. 11 is a block diagram of the process for semiconductor layer formation using the direct melting process. The first step 601 calls for measuring P-Type or N-Type semiconductor material in the proper proportion. At step 602 one melts the measured semiconductor material in carbon crucible. This is followed by step 603 of forming a mold cavity the thickness of finished layers from a mixture of fly ash, sand or other mold material with propylene glycol or atactic polypropylene solution. At step 604 the molten measured semiconductor material is poured into the mold. In step 605 the solution heated by the molten semiconductor material producing thick white fumes as the semiconductor material cools. After cooling, process step 606 is to remove the coated semiconductor material from mold. During process step 607 the cooled semiconductor material is cut into appropriate layer sizes.

Fig. 12 is a block diagram of semiconductor layer formation using the powdered metal process. Step 701 starts the process by measuring the P-Type or N-Type semiconductor material in the proper proportion. At step 702 one forms measured semiconductor layers under pressure into appropriate size and density of 90-98% using powder semiconductor material in the micro to nano size range. Step 703 subsequently sinters and anneals the layers in reducing atmosphere at a temperature of near melting temperature. Lapping, grinding or polishing of the layer surfaces is performed at step 704. This is followed at step 705 by annealing each layer in a reducing atmosphere. The next step 706 is optional calling for coating of the layer with metal ion diffusion barrier which is a coating of graphene. As in the other layer formation processes at step 707 the layer is coated using atactic polypropylene process of Fig. 14 or propylene glycol coating processes of Fig. 13. Lastly at process step 708 the coating is cured using the superconducting polymer curing process of Fig. 15.

Fig. 13 is a block diagram of the propylene glycol coating process. Step 801 calls for pouring propylene glycol into container approximately 1/8 to 1/4" deep. At step 802 a screen is set into the container suspended above the propylene glycol. The layers are then suspended on the screen that has been placed above the level of the propylene glycol at step 803. Step 804 calls for covering the container partially. At step 805 the container is heated until white fumes/mist fills the container. Step 806 calls for sustaining the fume/mist around the substrate for 20 minutes allowing propylene derivative to form and coat the substrate. This is followed by process step 807 calling for curing the coating using the superconducting polymer curing process of Fig. 15.

Fig. 14 is a block diagram of an atactic polypropylene coating process where atactic polypropylene heptane and dopant are supplied at step 900 followed in step 901 where the atactic polypropylene is dissolved in heptane. This is followed by step 902 where dopants are added to the solution. In step 903 dip, Spray coat, brush, sponge or any other application method to coat the layer with the solution. At step 904 one may apply Atactic Polypropylene solution to layer using any method. This is followed by process step 905 calling for curing the coating using the superconducting polymer curing process of Fig. 15.

Fig. 15 is a block diagram of a superconducting polymer curing process. The process starts with step 1001 where both sides of coated substrate or layer are exposed to UV light for one hour. (this step and following two steps may be combined or performed in any order). At step 1002 both sides of substrate or layer are exposed to microwave radiation for five minutes. Step 1003 heats the substrate or layer on hot surface to 100 deg. C for ten minutes. Lastly step 1004 cools the coated layer in air.

Fig. 16 is a block diagram for the electric field conditioning of the energy converter assembly to insure superconductivity and thermal contact between layers and coatings to insure superconductivity and low thermal resistance between layers and coatings. The process starts at step 1101 by connecting the negative terminal of a DC power supply or pulse width modulator to all of the hot layers and the positive terminal to all of the cold layers, placing the P-Type and N-Type semiconductors in a parallel electrical circuit. This is followed by step 1102 where the power source is energized for a time that is a function of the parameters of the apparatus to condition the conductive paths. The next step 1103 is to energize the power source with the terminals reversed for a time that is a function of the parameters of the apparatus to condition the semiconductor paths. Lastly at step 1104 one is to confirm conditioning of entire apparatus by measuring its conductivity with the parallel circuit removed.

Fig. 17a shows a timing diagram of the operation of the switching mechanism106 shown in Fig. 6b of the preferred embodiment of the present invention. Element 1201 represents the period t1, that the stack 105 is connected to the load 103 through conductor 112 and conductor 104. 1202 represents the period t2, that the stack 105 is connected to the load 103 through conductor 113 and conductor 104 and to is a period when stack 105 is connected to the load 103 through conductors 112, 113 and 104 and is referred to as an overlap. It can be seen that 1203 represents another period t3 that the stack 105 is connected to the load 103 through conductor 112 and conductor 104 with another overlap to.

Fig. 17b shows an alternative timing diagram of the operation of the switching mechanism 106 shown in Fig. 6b. In this mode of operation 1204 represents the period t4, that the stack 105 is connected to the load 103 through conductor 112 and conductor 104. 1206 represents the period t6, that the stack 105 is connected to the load 103 through conductor 113 and conductor 104. 1205 represents a period t5 when stack 105 is in a quiet period not being connected to neither conductor 112 nor 113.

Fig. 18 is a block diagram of a process for coating layers with superconducting paste. The process starts with step 1301 where a supply of a particulate dopant is attained. At step 1302 one gains a supply of polymer in solution. This is followed by step 1303 of mixing the particulate and solution to form a paste. At step 1304 one applies the paste to all or part of a layer. This is followed by step 1305 where two or more layers are assembled mechanically.

The layers are then heated at step 1306. Step 1307 finishes the process by applying DC voltage to assembled layers during heating.

Fig. 19 is a block diagram of coating layers using the electro-deposition process for coating of superconducting polymers. The process starts by supplying the layers at step 1401 followed by supplying an electrical and polar magnetic cell for coating at step 1402. Step 1403 calls for submerging the layer to be coated in dissolved monomer or polymer. A voltage is applied across the cell at step 1404 in the presence of a polar magnetic field across the cell at step 1405. The coated layer is removed from the cell at step 1406.

Fig. 20 is a block diagram for the process of superconducting polymer coating assembled layers. The first step 1501 is to supply assembled layers and supply electrical and magnetic cell for coating at step 1502. This is followed by step 1503 of submerging the assembled layers in dissolved monomer or polymer. Step 1504 requires applying a voltage across the cell while applying a polar magnetic field across the cell to satisfy step 1505. Lastly the coated and assembled layers are removed from the cell at step 1506.

Fig. 21 is a block diagram for superconducting polymer coated semiconductor layer formation of the preferred embodiment of the present invention. The process starts with step 1601 where P-Type or N-Type semiconductor material are in the proper proportion, followed by step 1602 where a supply of a solution of a polymer, solvent and dopant is obtained. Step 1603 begins the molding process by forming a carbon mold cavity the thickness of finished layers as seen in Fig. 24a and 24b at reference numbers 1903. Step 1604 calls for Insulating the contact edges of the mold as shown in Fig. 24a and 24b at reference number 1907. In step 1605 the polymer from step 1602 is applied to the separated mold hales 1901 and 1905 followed by step 1606 where the mold is assembled as in Fig. 24b and the two halves are held together with a clamp that is not shown. In step 1607 the mold halves are connected to a supply of electricity while at step 1608 the semiconductor material from step 1601 is melted in a carbon crucible. Subsequently, at step 1609 the molten semiconductor material is poured into the mold cavity through the opening shown in Fig. 24b at reference number 1904. The operator can now observe that electricity is passing through the superconducting polymer coated cast wafer at step 1610 after which the mold can be disassembled to extract the superconducting polymer coated semiconductor layer at step 1611.

Fig. 22 is a block diagram of the process that activates the superconductivity of the doped polymer or polymer coated layers. The process starts by supplying the doped polymer coated layers at step 1701. Step 1702 calls for supply of the required equipment including a UV light source, polar magnet 1703 and microwave source 1704 respectively. Steps 1705, 1706 and 1707 that call for exposing the layers to UV light, a polar magnetic field and microwave radiation may be performed separately in any order or together simultaneously.

Fig. 23 is a block diagram of process for further activating the superconductivity in polymer or doped polymer coated layers. This process starts at step 1801 to supply assembled layers. Steps 1802 and 1803 call for supplying a heat source directed towards the hot layers and supplying a heat sink directed towards the cold layers respectively. At step 1804 a pulsating DC current is connected across the layer electrical connections by a DC power supply or pulse width modulator a capacitive discharge or some other high current pulse, for example. As a result. step 1805 will cause Ionized polarons to cross and connect between P-Type and N-Type semiconductors carrying electrons through the polymer. Per step 1806 the polymer coating will impede phonons flow violating the Wiedemann - Franz Law per step 1807 the pulsating current accelerates electron flow making superconducting polymer threads. Subsequently in step 1808 the electrons separate from phonons enhancing the voltage and current flow from the layers which in turn per step 1809 the enhanced flow of electrons triggers Peltier, magneto-caloric and electro-caloric effect causing cold layer to be cool. The last step 1810 produce an increased temperature difference across the semiconductor layers increases Seebeck effect yielding higher voltage and current output.

Fig. 24a shows a two piece mold made form carbon blocks. The base of the mold 1901 has a cavity 1902 that is machined in the shape and depth 1903 of a semiconductor layer of the preferred embodiment of the present invention.

The base also has a chamfered edge 1904 leading to the top edge of the cavity 1902. The top of the mold is made of a carbon block of similar dimensions to the base and has a flat inside surface 1906. The top 1905 and the base 1901 are separated by a thin electrical insulator 1907.

Fig. 24b shows the mold components of Fig 24a assembled and ready for pouring of the molten semiconductor melt. The base 1901 and top 1905 are separated by and in intimate contact with the insulator 1907. The mold components are held in this position by a clamp (un-shown) and the molten semiconductor material (un-shown) is poured into the cavity 1902 through the chamfer 1904 of 19a.

Fig. 25 is a block diagram for installing a cryogenic member for applying pressure to a thermoelectric stack resulting in improved thermal and electrical conduction between layers. This process requires a cryogenic cooling source operating at cryogenic temperature at step 2001 and a thermoelectric stack requiring application of pressure to improve contact between layers at step 2002.

A cryogenic treatable member made of shape memory materials is called for having a smaller inner dimension (between the headed ends) than the outer dimension of the thermoelectric stack at step 2003. Step 2004 calls for cooling the cryogenic treatable member to cryogenic temperature in the cryogenic cooling source. At this point a mechanical device for stretching members at step 2005 is used to stretch the cryogenic treatable member to a larger inner dimension than the outer dimension of the thermoelectric stack at step 2006.

Quickly removing the cryogenically treatable member from the cryogenic cooling source at step and assembling it around the thermoelectric stack before an appreciable member temperature rise completes step 2007. The assembly is completed at step 2008 where the cryogenically treatable member is allowed to warm to room temperature causing shrinkage of the member thereby applying pressure to the thermoelectric stack. .

Fig. 26a shows a thermoelectric stack 5 from Fig. 6a and Fig. 6b. Two spanner plates 2101 are positioned one at the top and one at the bottom of the thermoelectric stack 5. The top and bottom of the stack 5 is electrically insulated from the spanner plates 2101 by insulation layers 2104. The two cryogenically treatable members 2102 are shown in their stretched cryogenically cold condition.

Fig. 26b shows the thermoelectric stack 5 after assembly with the two spanner plates 2101 being pressed towards each other by the cryogenic members 2103 that have shrunk due to warming to room temperature. From 5,000 to 30,000 psi pressure can be developed in the layers of the stack 5 promoting intimate contact and very low electrical resistance.

All the features disclosed in this specification, including any accompanying abstract and drawings, may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

Claim elements and steps herein may have been numbered and/or lettered solely as an aid in readability and understanding. Any such numbering and lettering in itself is not intended to and should not be taken to indicate the ordering of elements and/or steps in the claims.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiments have been set forth only for the purposes of examples and that they should not be taken as limiting the invention as defined by the following claims. For example, notwithstanding the fact that the elements of a claim are set forth below in a certain combination, it must be expressly understood that the invention includes other combinations of fewer, more or different ones of the disclosed elements.

The words used in this specification to describe the invention and its various embodiments are to be understood not only in the sense of their commonly defined meanings, but to include by special definition in this specification the generic structure, material or acts of which they represent a single species.

The definitions of the words or elements of the following claims are, therefore, defined in this specification to not only include the combination of elements which are literally set forth. In this sense it is therefore contemplated that an equivalent substitution of two or more elements may be made for any one of the elements in the claims below or that a single element may be substituted for two or more elements in a claim. Although elements may be described above as acting in certain combinations and even initially claimed as such, it is to be expressly understood that one or more elements from a claimed combination can in some cases be excised from the combination and that the claimed combination may be directed to a subcombination or variation of a subcombination.

Insubstantial changes from the claimed subject matter as viewed by a person with ordinary skill in the art, now known or later devised, are expressly contemplated as being equivalently within the scope of the claims. Therefore, obvious substitutions now or later known to one with ordinary skill in the art are defined to be within the scope of the defined elements.

The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptually equivalent, what can be obviously substituted and also what incorporates the essential idea of the invention.

What is claimed is:

1. An assembly having a graphene diffusion barrier comprising:

a first metal or semiconductor;

a second metal or semiconductor; and

a layer of graphene disposed between the first metal or semiconductor and the second metal or semiconductor.

2. The assembly of claim 1, wherein the first metal or semiconductor is a first semiconductor and the second metal or semiconductor is a second semiconductor.

3. The assembly of claim 2, wherein the assembly is a semiconductor chip.

4. The assembly of claim 3, wherein the semiconductor chip is a CMOS chip.

5. The assembly of claim 1, wherein the graphene includes a carbon donating material.

6. The assembly of claim 1, wherein the first metal or semiconductor is a carbon absorbing material.

7. The assembly of claim 1, wherein the graphene is formed from a polymer by heating.

8. The assembly of claim 6, wherein the carbon absorbing material is an iron containing material.

9. The assembly of claim 8, wherein the carbon absorbing material is an iron / nickel alloy.

10. The assembly of claim 6, wherein the carbon absorbing materials are selected from the group consisting of silicon dioxide, a copper substrate, an iron substrate, and an iron/nickel substrate.

11. The assembly of claim 5, wherein the carbon donating material is selected from the group consisting of carbon, carbon nano-ribbon, graphene, carbon nano-tubes, and carbon impregnated metals, ceramics, polymers, sintered metal, powdered metals, alloys, and composites.

12. A method for providing a diffusion barrier between first and second materials, comprising:

providing the first material and a second material to be interconnected;

contacting a carbon donating material with at least one of the first material and the second material;

applying a pressure to an assembly of the first material and the second material with the carbon donating material therebetween; and

heating the assembly to a temperature below a melting point of each of the first material and the second material to cause a bond to form from carbonization of the carbon absorbing material, wherein the carbon absorbing material forms a diffusion barrier.

13. The method of claim 12, wherein at least one of the first material and the second material is an iron containing material.

14. The method of claim 13, wherein the iron containing material is an iron / nickel alloy.

15. The method of claim 12, wherein the heating step is performed in an inert atmosphere.

16. The method of claim 12, wherein at least one of the first material and the second material are selected from the group consisting of a semiconductor, silicon dioxide, a copper substrate, an iron substrate, and an iron/nickel substrate.

17. The method of claim 12, wherein the carbon donating material is selected from the group consisting of carbon, carbon nano-ribbon, graphene, carbon nano-tubes, and carbon impregnated metals, ceramics, polymers, sintered metal, powdered metals, alloys, and composites.

18. A 2-dimensional direct graphene deposition-based method for forming an electrical interconnect with a diffusion barrier between , comprising:

providing a nickel metal on a substrate;

layering graphene onto the nickel metal;

applying a pressure to an assembly of the graphene and the nickel metal;

heating the assembly to cause the graphene to defuse through the nickel metal to coat the substrate in a smooth layer; and

removing the nickel metal, wherein the graphene acts as a diffusion barrier on the substrate.

19. The method of claim 18, further comprising removing the nickel metal by etching.

20. The method of claim 18, wherein the substrate is selected from the group consisting of a silicon, tungsten, ruthenium and cobalt.

ABSTRACT

There are two parts to build fusion carbon metal interconnects. First are the fusing metals/alloys, typically in the Martensite phase and lacking carbon. Second are carbonized materials that have carbon infused. These carbonized materials may be referred to as carbon donating materials. Both parts can be interchanged as the substrate or mounted component, or the parts can form linear interface connections. The finished interfaces have very low electrical resistance and/or zero interface electrical resistance. The interconnect circuit topography materials and connections are endless and is dependent on circuit design. One example of such interface is a solderless thermoelectric device capable of use at higher operating temperatures as compared to conventional low temperature solders thus allowing the thermoelectric device to be used in a Seebeck device, for example. Another example is the use for bonding microcircuits using fusion and/or surface absorption of carbon.